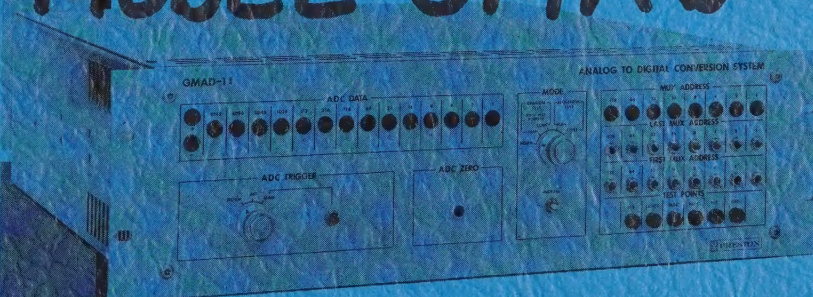


GM SERIES
ANALOG-TO-DIGITAL CONVERSION
SYSTEMS

P/N 58700
MODEL GMAD-1



— ADC ZERO —



GM SERIES

MULTIPLEXING, ANALOG-TO-DIGITAL
CONVERSION SYSTEM

PART NUMBER 58700

MODEL NUMBER GMAD-1

SERIAL NUMBER RAA-434



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INTRODUCTION

This book contains instructions for the operation and maintenance of the Preston GM Series Multiplexing Analog-to-Digital Conversion System. Information including the functional description and theory of the multiplexer and the Analog-to-Digital Converter is contained in specific sections. System control and operation including calibration and trouble-shooting are also covered by separate sections.

The GM Series Multiplexing Analog-to-Digital Conversion System will accept a quantity of individual analog signals, sample each one and produce a binary representation of each analog signal. Control of the channel selections and conversion process may be done manually, externally controlled by computer, or may be accomplished by an optional internal timing and sequencing network.

Description of Multiplexer and Converter Control methods may be found in Section 1 and Section 3. Specific timing and control information may be found in the Factory Test Report, Section 10. Sections 2 and 4 contain information on the functional building blocks of the system and Section 5 provides specific information relative to the building blocks (i.e. type of multiplexer, logic number of channels, etc.) which make up your system. We would suggest a thorough review of Sections 5 and 10 of this manual before proceeding to initiate the interface and turn-on procedures illustrated in this document.

A complete replacement Parts List is included along with all drawings and schematics pertaining to your specific system. Prices quoted in the Parts List are subject to change. The minimum order is \$25.00.

(continued)

The Part Number which describes this system is located on the rear panel of the Card Module (or modules). This part number describes this instrument completely and should be referenced in all correspondence.

Should the system need to be returned to Preston for repair or rework, the item should be sent to the Anaheim plant, Attention: Customer Service, shipping prepaid. Also, include reasonably complete information concerning the nature of the failure or your reason for the return of the equipment.

Our address is:

PRESTON SCIENTIFIC INC.
805 East Cerritos Avenue
Anaheim, California 92805

Our Telephone is: (714) 776-6400

If there are any questions concerning our product, please contact our Customer Service Department.

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SECTION 1

SYSTEM INTERFACE AND CONTROL

1.1 BASIC OPERATION INSTRUCTIONS

The Preston Multiplexing Analog-to-Digital Conversion System has a power requirement of 110/220 volts AC 50-60 Hz. The specific prime power voltage requirement is customer specified and is noted both in the Drawing Section and the Test Report.

The GM System card modules are designed to be mounted into a standard 19-inch RETMA Relay Rack. To prevent damage to the front panel, nylon filler washers should be placed under the rack mounting screws. For correct weight distribution, drawer slides must be used for support. The unit has an integral fan; ambient air should be maintained at less than 50°C.

Unless otherwise specified the prime power is controlled by a Rear Panel ON-OFF Switch and fuse. The value of the fuse is noted on the rear panel and also in the Parts List.

1.2 ANALOG INPUT TERMINATIONS

Two types of multiplexers are employed by the GM Series System. The Model GMM Multiplexer is a single-pole single-throw FET type commutator. The Model GMM is normally used for single-ended multiplexing applications. Some systems are configured using two GMM switches on each channel to provide a differential multiplexing capability.

1.2 ANALOG INPUT TERMINATIONS (continued)

The Model GMD series Amplifier-Multiplexers provides a differential amplifier per channel multiplexer capability for applications which demand intra-channel isolation. The Model GMD may be operated single-ended or differential depending upon the requirements of the customer.

1.2.1 Single-Ended Input Model GMM

When the Model GMM Multiplexer is used for single-ended applications, the input signal is connected between the channel input and analog ground (shield). The rear connector provides terminations for both of these connections for each channel. Please refer to the customer connection drawing in Section 9 and to the source and/or input impedance specifications for the multiplexer.

1.2.2 Differential Input Model GMM

Differential Input using the GMM Multiplexer is accomplished by using a pair of single-ended input multiplexer switches on each channel (please refer to the customer connection drawing for input termination pin locations). You will note upon referring to the customer connection drawing, that the differential input is carried on three wires HI, LO, and SHIELD. The Shield is not electrically terminated at the multiplexer switch, but does physically surround the input circuitry. The Shield must be referenced to the Common Mode Source. The impedance between the HI or LO wires and multiplexer ground must not exceed the allowable specified source impedance of the multiplexer.

1.2.3 Differential Input Model GMD

The input to the Model GMD Multiplexer is designed to be either differential or single-ended. The differential input uses a three terminal input, i.e. HI, LOW and SHIELD, and all terminations are available at the rear connector. The SHIELD is not connected internally, but does physically surround the input section of the multiplexer channel. The SHIELD must, however, be referenced to the Common Mode Source. The impedance between the HI or LOW wires and GMD ground must not exceed 10 megohms.

1.3 DIGITAL INPUT AND OUTPUT LINE TERMINATIONS

1.3.1 Input Control Line (Figure 1.1) Terminations

Input Control Line receiving devices are normally TTL Logic, 74 series integrated circuits. These control lines are normally not internally terminated and for this reason, we recommend series termination resistors of 33 ohms at the driving end as shown in Figure 1.1

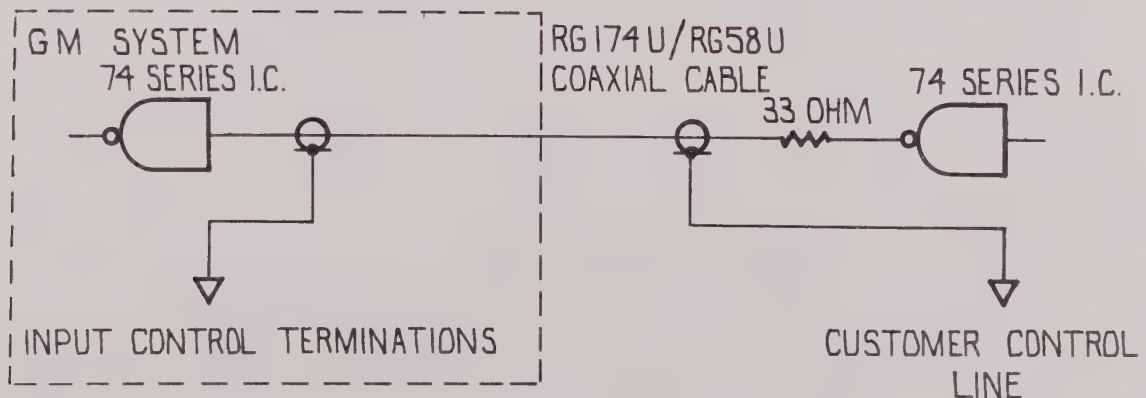


FIGURE 1.1

1.3.2 Output Control and Data Lines (Figure 1.2) Terminations

The logic used as drivers for the output control and the digitized data lines are TTL 74 Series integrated circuits. These lines are internally provided with a 33 ohm series resistor per line and are designed to drive a 50 ohm impedance coaxial cable, typically either #RG174U or #RG58U (See Figure 1.2).

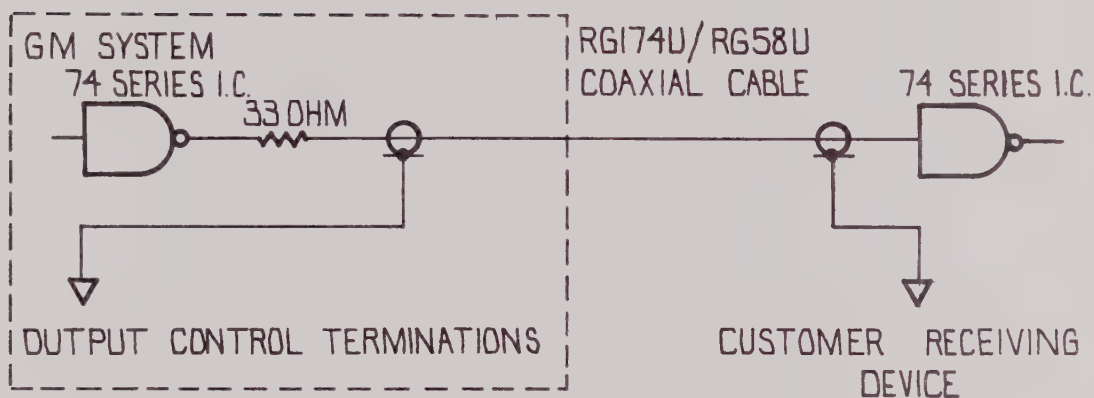


FIGURE 1.2

1.4 SYSTEM CONTROL

Control of the MUX/ADC System may be accomplished by any one of the following methods.

- 1.4.1 All External Control (without optional GMC Logic Control Package)
Control signal input connections are provided for (1) Binary channel address, no storage, (2) Sample-and-Hold commands (when applicable) and (3) Direct Trigger ADC (DTADC). When this method of control is used, all operations of the MUX/ADC combination are controlled by external means, all necessary settling times must be observed, and the channel addressing must not change during the conversion process. A timing diagram is supplied in Section 9 and contains the necessary information for the specific control signals and their proper timing sequence.
- 1.4.2 Control Using an External Clock (with optional GMC Logic Control)
For a complete description of the Optional GMC Logic Control refer to Section 3 of this Manual.

The optional GMC Logic Control Package permits the system to be operated in the external mode by either of the following two methods. In the external (NORMAL) Mode, a channel may be randomly addressed. When the ADD-X signal is HI initiation of a CLOCK pulse will select the desired channel and after the proper delays will command the ADC to start the conversion process. No external Direct TADC is required.

1.4.2 (continued)

Also in the external mode (NORMAL Mode), the front panel select switches of the GMC Control Logic are used to establish the first and last channels of a sequence of channels. When the ADD-X signal is L0 and each clock pulse is received (externally provided), the next channel in sequence will be selected followed by an automatic initiation of the conversion process. No external Direct TADC is needed in this mode.

1.4.3 System Control (with GMC Logic Control Package)

The following are some of the methods for system control via the Front Panel:

- (a) Repetitious selection and conversion of the same channel by:
 - . . . placing the First MUX Address Switches on the desired channel
 - . . . placing the Mode Switch in RANDOM/MAN
 - . . . pressing the Manual Pushbutton (Multiplexer Control)
 - . . . placing the ADC/Trigger in INT (Internal).

As a result of the foregoing "set-up" the ADC will repetitively digitize the selected channel at a rate governed by the ADC Internal Clock (usually to 10 Hz).

1.4.3 (continued)

(b) Repetitious conversion of the same channel may also be accomplished by:

- . . . placing the Mode Switch in RANDOM/CONT (continuous)
- . . . placing the First MUX Address switches in the desired channel
- . . . placing the ADC/trigger in the NORMAL position

As a result of this "set-up", the ADC will repetitively digitize the selected channel at a rate governed by the Multiplexer Clock (usually at the maximum repetition rate of the converter/multiplexer combination).

(c) Repetitious conversion of the same channel "manually" is accomplished by:

- . . . placing the First MUX Address switches on the desired channel
- . . . placing the Mode Switch in the RANDOM/MAN position
- . . . Pressing the Manual Pushbutton (Multiplexer Control)
- . . . Placing the ADC/Trigger in MAN

In the preceding configuration, the ADC will digitize the selected channel each time the Manual pushbutton (ADC Control) is depressed.

(d) Sequential Operation

Sequential selection and conversion of a series of channels manually by:

- . . . placing the Mode Front Panel Switch in SEQUENTIAL/MAN position
- . . . placing the First MUX Address switches to the first channel desired
- . . . placing the Last MUX Address switches to the last channel desired

- . . . placing the ADC/trigger in the NORMAL position

1.4.3 (con tinued)

In this "set-up" pressing the Manual button (Multiplexer Control) will select each channel one at a time and convert that channel.

(e) Sequential selection and conversion of a series of channels automatically by:

- . . . placing the Mode Switch in the SEQUENTIAL/CONTINUOUS position
- . . . placing the First MUX Address switches to the first channel desired
- . . . placing the Last MUX Address switches to the last channel desired
- . . . placing the ADC/Trigger in the NORMAL position

The preceding allows the control system to advance through and convert each channel in sequence at a rate governed by the multiplexer control clock (usually at the maximum repetition rate of the Multiplexer/ADC combination).

1.5 SAMPLE-AND-HOLD CONTROL LOGIC

Each one of the sample-and-hold boards has its own control logic. The logic diagram is pictured in Figure 1.3. Refer to the chart in Figure 1.4 for the different ways to control the sample-and-hold modes and their subsequent logic connections.

Common types of control are:

- (a) A pulse on the sample line to obtain the sample mode, and a pulse on the hold line to obtain the hold mode
- (b) Single line drive sample logic line; true for sample, false for hold
- (c) Single line drive, hold logic line; true for hold, false for sample.

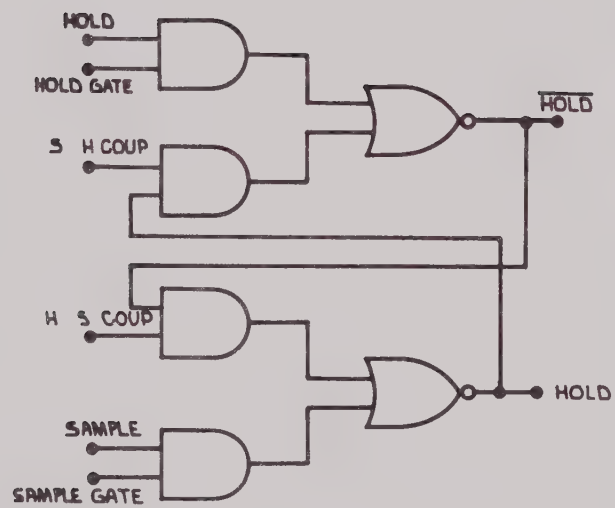


FIGURE 1.3

	HOLD	HOLD GATE	SH COUP	SAMPLE	SAMPLE GATE	HS COUP
PULSE TO SAMPLE PULSE TO HOLD	D	T	T	D	T	T
	T	D		T	D	
DRIVE TRUE FOR SAMPLE	X	0	T	D	T	F
	0	X		T	D	
DRIVE TRUE FOR HOLD	D	T	F	X	0	T
	T	D		0	X	

X = UNUSED

0 = KEPT AT LOW LOGIC LEVEL

T = TRUE

F = FALSE

D = DRIVE

Figure 1.4

SECTION 2

MULTIPLEXER

2.1 FUNCTIONAL DESCRIPTION (Figure 2.1)

The GMM Multiplexer is a single-ended input/single ended-output semiconductor device. Some systems use this device as a differential multiplexer by using a pair of GMM Multiplexer switches for each differential channel involved followed by either a differential buffer or Sample-and-Hold Amplifier.

Figure 2.1 is an over-all block diagram of the GMM Multiplexer in a system application. Analog input signals are connected to the multiplexer channels from the rear connectors by shielded cabling. Each multiplexer circuit board contains four multiplexer switches, associated switch drive control logic, and analog overload clamps.

Control of the multiplexer may be directed from the front panel (Optional GMC Logic Control Package, see Section 3 and Figure 2.1 or by the customer interface at the rear panel connectors (refer Section 1).

2.2 SPECIFICATIONS

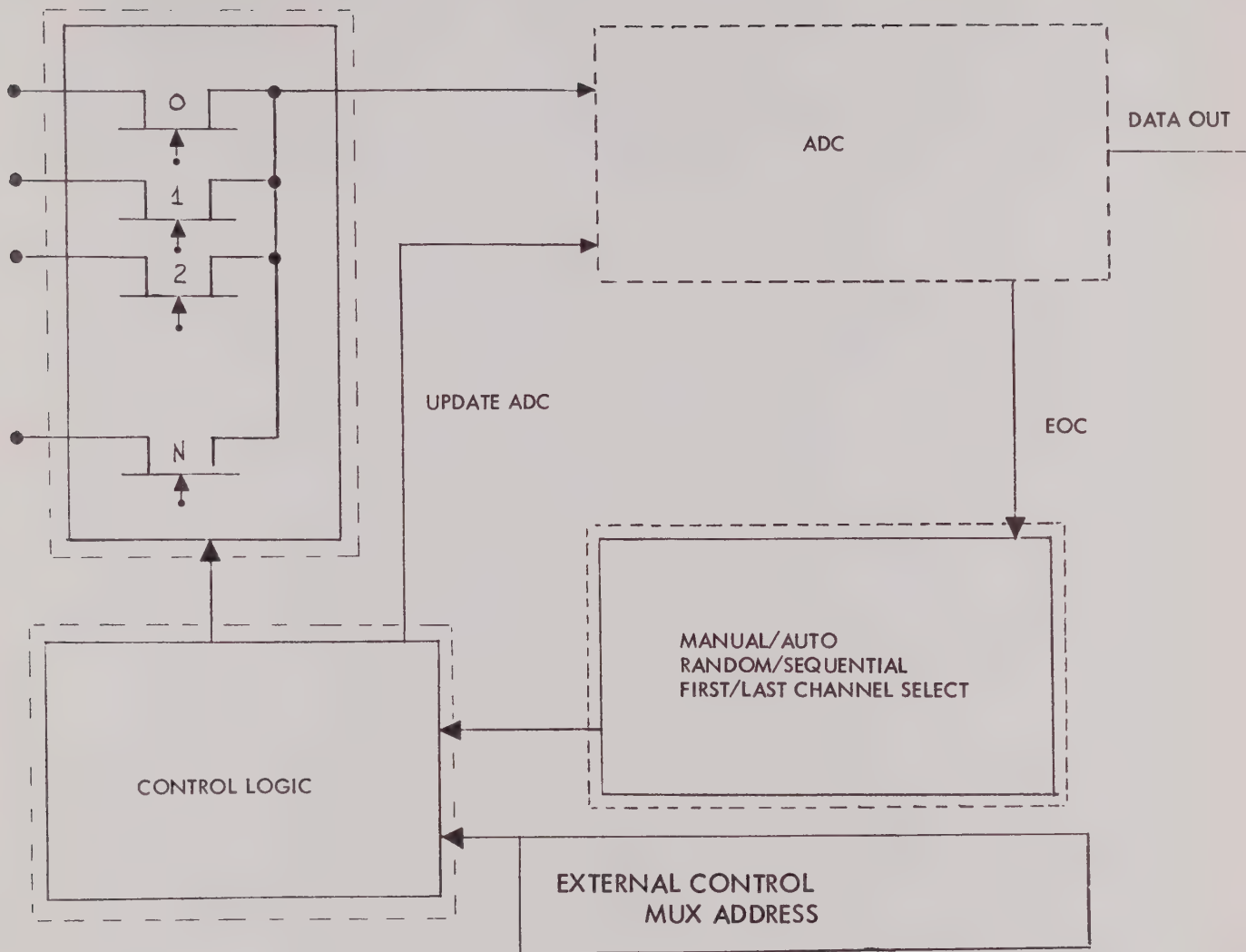
2.2.1 Type: Single-ended SPST

2.2.2 Channel Selection: Selection by random address, sequential or any combination of both, when the GMC Logic Control Package is employed

2.2.3 Switching Time: Less than 1 microsecond.

2.2.4 Accuracy: 0.01%

- 2.2.5 Input Impedance: Greater than 50 megohms
- 2.2.6 Crosstalk: Between channel crosstalk is less than 0.01% of full scale.
- 2.2.7 Linearity: 0.01% of full scale.
- 2.2.8 Zero Drift: Less than ± 1.0 millivolt.
- 2.2.9 Logic Levels: Either positive or negative true.



DOTTED LINES INDICATE THE MULTIPLEXER AND ITS CONTROLS
MAY BE MOUNTED IN THE SAME MODULE AS THE ADC OR MOUNTED
IN A SEPARATE MODULE DEPENDING UPON CUSTOMER REQUIREMENTS

FIGURE 2.1

MULTIPLEXER MODULE BLOCK DIAGRAM

2.3 OPERATING INSTRUCTIONS

The System Multiplexer may be totally external controlled by the customer or may be controlled by the Optional GMC Logic Control Package. A description of these control methods appears in Sections 1 and 3 of this manual.

2.4 THEORY (Figure 2.2)

The multiplexer switch is a Field Effect Transistor (FET).

Figure 2.2 shows channel address circuit and a FET switch circuit.

Each of the GMM Multiplexer boards contain four identical FET switch circuits; one for each of the four channels. Because the FET has no inherent offset voltage, whatever signal is on the input will also appear on the output (when the switch is turned ON). One characteristic of the FET used in the GMM Multiplexer is that it is normally ON with zero gate voltage and is turned OFF by the application of a voltage having negative polarity.

Also shown in Figure 2.2, the analog channel input is connected to the Drain (D) and the multiplexer output is connected to the Source(S) of the FET. When the voltage between the Drain and the GATE (G) is Zero, the FET will conduct and the Source will be brought to the potential of the Drain.

To turn off the FET, the Gate must be clamped to a negative voltage.

To insure that the Gate will obtain the same potential as the Drain and the FET will turn on in the shortest amount of time when the Gate is released, the input of a unity gain amplifier (see Figure 2.3) is tied to the Drain of the FET and the output of the unity gain amplifier is tied to the Gate of the FET. This added circuit increases the slewing rate of the FET Gate.

The multiplexer switch and its unity gain amplifier appear in Block Diagram Form in Figure 2.4

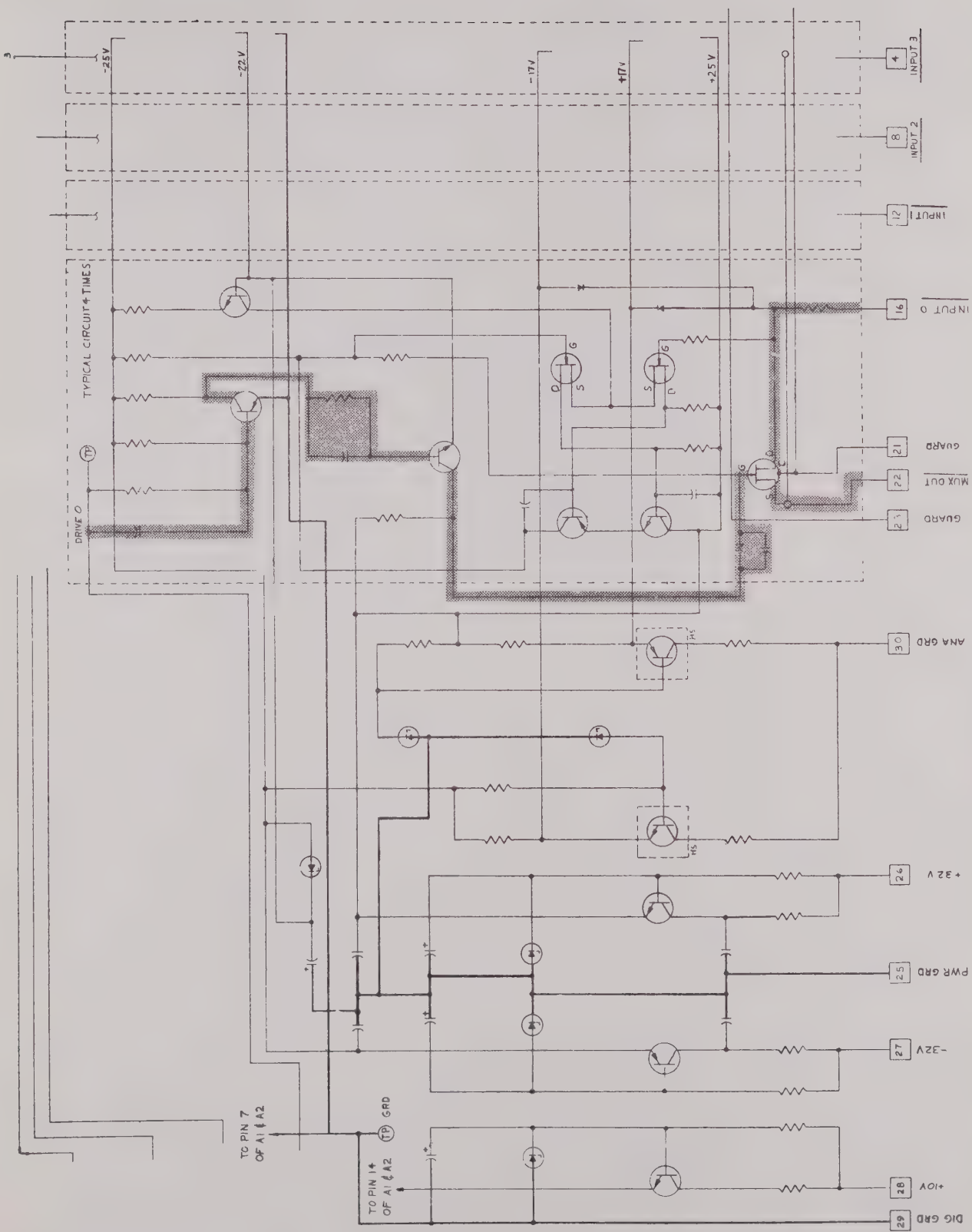


FIGURE 2.2
MULTIPLEXER SWITCH

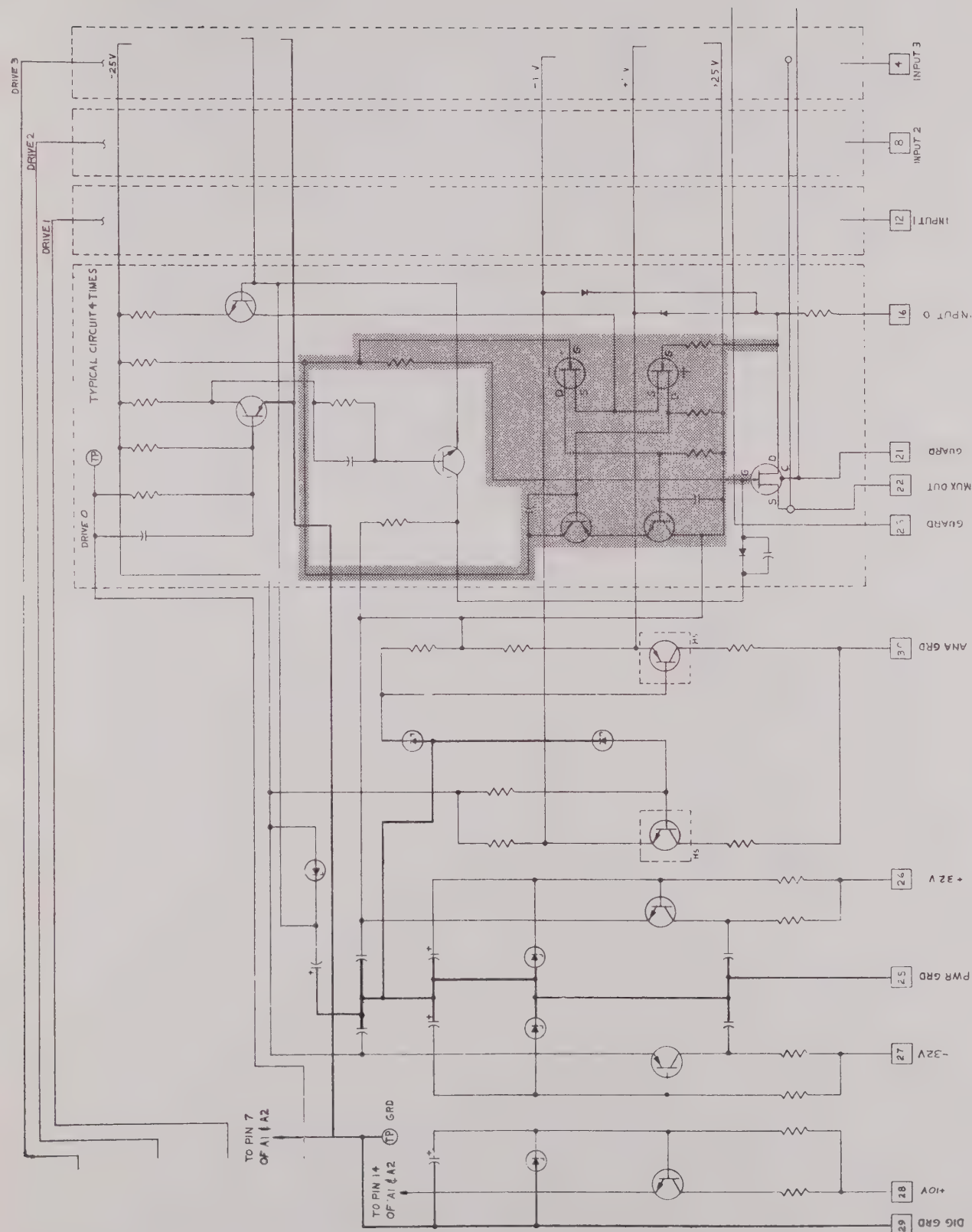


FIGURE 2.3
UNITY GAIN AMPLIFIER

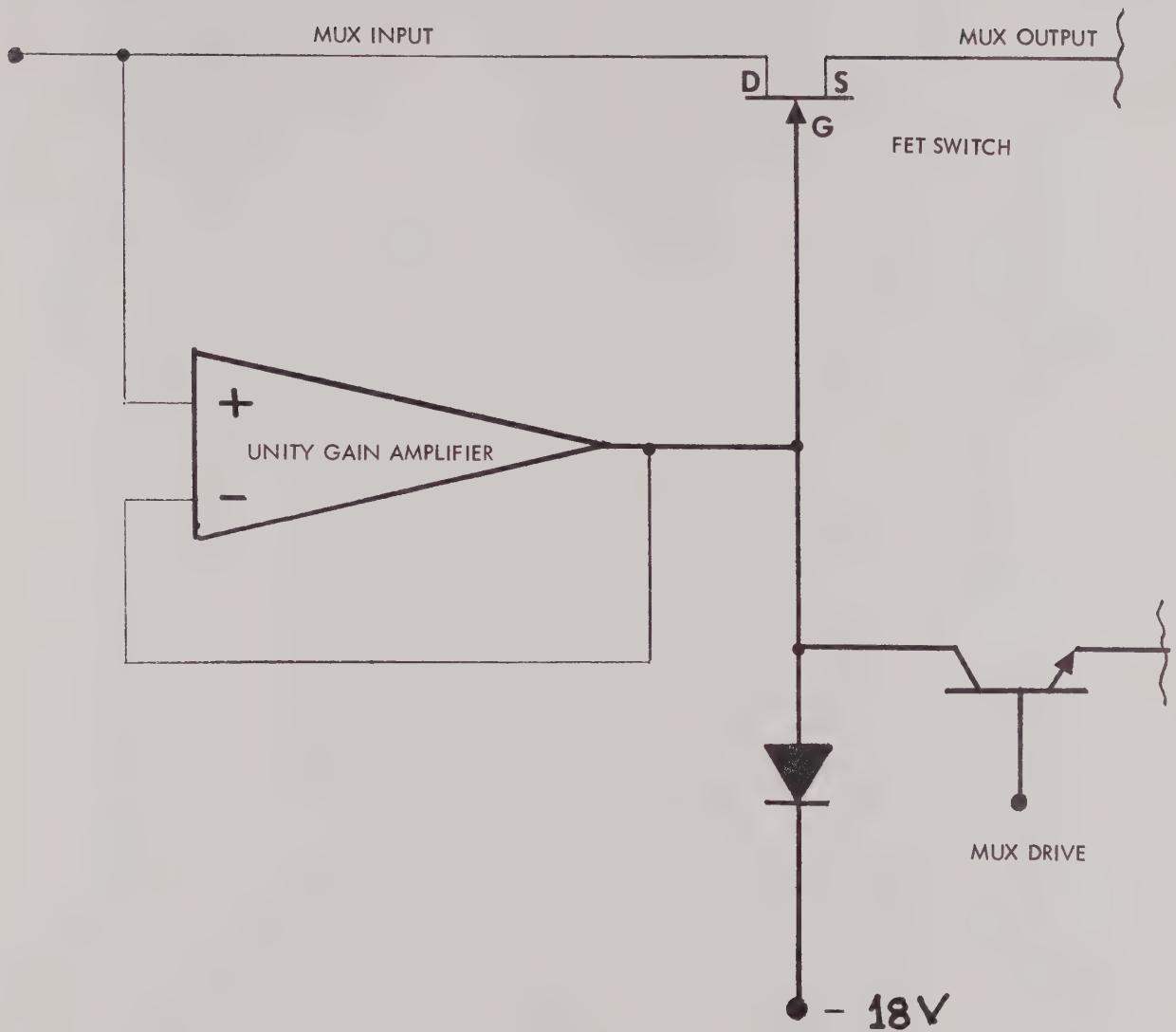


FIGURE 2.4

MULTIPLEXER SWITCH BLOCK DIAGRAM

2.5 FUNCTIONAL DESCRIPTION MODEL GMD

The Model GMD Amplifier Multiplexer is a differential input amplifier followed by a single-ended input/single-ended output semiconductor switch.

Figure 2.5 is an overall Block Diagram of the Model GMD Multiplexer in a system application. Analog signals are connected to the multiplexer channels by shielded cabling. Each multiplexer board may contain one or two multiplexer channels, associated drive control logic and analog overload clamps. The number of channels per circuit board is determined by the particular system application.

Control of the multiplexer channels may be directed from the front panel (Optional GMC Logic Control Package, see Section 3 and Figure 2.5) or by the customer interface at the rear panel connectors (refer to Section 1.)

2.6 SPECIFICATIONS

2.6.1	Amplifier Type	Direct coupled fixed gain
2.6.2	Gain	The gain of the amplifier is fixed single gain between 1 and 5 for the Model GMD-1 and at one-tenth (0.1) for the Model GMD-01.
2.6.3	Gain Accuracy	$\pm 0.01\%$ of full scale
2.6.4	Gain Stability	$\pm 0.01\%$ of full scale for six months at the same temperature
2.6.5	Gain Temperature Coefficient	Less than $\pm 0.002\%$ per degree C
2.6.6	Gain Trim	Permits adjustment to within 0.01%; resolution is 0.005% or better
2.6.7	DC Linearity	Maximum deviation $\pm 0.01\%$ of full scale

2.6.8	Zero Stability	Short term ± 0.5 millivolts RTO (Relative to Output) for 48 hours at the same temperature.
2.6.9	Zero Temperature Coefficient	± 0.05 millivolts RTO per degree C
2.6.10	Zero Trim	A zero offset adjustment is provided with resolution of 0.1 millivolts
2.6.11	Input Impedance	100 megohms for the Model GMD-1, 100 k ohm for the Model GMD-01
2.6.12	Shunting Capacitance	100 picofarads
2.6.13	Common Mode Rejection	80 db from DC to 60 Hz
2.6.14	Common Mode Voltage*	10 volts peak-AC or DC for balanced inputs, 5 volts peak for single-ended inputs
2.6.15	Pumpout Current	10 picoamps nominal
2.6.16	Input Connection	Requires only three wires: Input High, Input Low and Guard.
2.6.17	Input Overload Recovery*	The amplifier will recover from an overload of two times full scale to within $\pm 0.05\%$ of full scale in less than 200 microseconds. Recovery time of the amplifier increases proportionately as the bandwidth decreases (i.e., at 1 kHz, recovery time is 2 milliseconds).
*The voltage levels referenced in these specifications should be multiplied by 10 when applied to the GMD-01 Amplifier-Multiplexer.		
2.6.18	Output Multiplexed**	Commutated ± 10 volts full scale

**A Direct Output of the GMD Amplifier is available upon special request. This output is electronically located before the MUX Switch input.

2.6.19	Output Impedance-ON	500 ohms maximum
2.6.20	Output Leakage Current-OFF	15 nanoamps maximum
2.6.21	Crosstalk	0.01% of full scale maximum for 100 channels.
2.6.22	Switching Time	1 microsecond to 0.01% of full scale into a load of 10 megohms shunted by 500 pf (analog buss should be guarded and driven externally if wiring capacity exceeds 500 pf or if insulation exhibits dielectric absorption).
2.6.23	Fault Condition	The multiplexer switch is protected against fault condition of the amplifier.
2.6.24	Bandwidth	Less than 3 db down at 1 MHz at 10 volts peak-to-peak.
2.6.25	Optional Filter	Any fixed bandwidth from 10 Hz to 1 MHz
2.6.26	Settling Time	2.0 microseconds maximum to within 0.01% of final value ± 10 microvolts RTI at 1 MHz. Settling time of the amplifier increases proportionately as the bandwidth decreases (i.e. at 1 kHz, settling time is 2 milliseconds).
2.6.27	Noise Characteristics	Output noise is less than 1.0 millivolts peak-to-peak; typically 0.5 millivolts peak-to-peak.

2.7 OPERATING INSTRUCTIONS

The System Multiplexer may be totally controlled by the customer or may be controlled by the Optical GMC Logic Control Package. A description of these control methods appear in Sections 1 and 3 of this manual.

2.8 THEORY (Figure 2.6)

The Multiplexer Switch is a Field Effect Transistor (FET). Figure 2.6 shows the channel address circuit and the FET switch circuit. Because the FET has no inherent offset voltage, whatever signal is on the input will also appear on the output (when the switch is ON). One characteristic of the FET used in the Model GMD Amplifier Multiplexers is that it is normally ON with ZERO GATE voltage and is turned OFF by application of a voltage having negative polarity.

Also shown in Figure 2.6, the output of the GMD Amplifier is connected to the DRAIN (D) and the multiplexer output is connected to the source(s) of the FET. When the GATE is released from its negative potential and assumes the potential of the DRAIN, the FET will turn ON and the source will be brought to the potential of the DRAIN.

The Multiplexer Switch and its input amplifier appear in block diagram form in Figure 2.7.

2.9 CALIBRATION

2.9.1 Common Mode adjustment

- (a) Tie the input HI and input LO together.
- (b) Apply a 20 volt, 60 Hz, AC signal source between the tied-together inputs and ground.
- (c) Observe the test point marked AMP OUT. Adjust the CM potentiometer for minimum output (20 millivolt scale).

2.9.2 ZERO

Short the input of the multiplexer and adjust the ZERO potentiometer for a zero reading on the ADC readout (within the accuracy of the system).

2.9.3 GAIN

Regardless of the Gain of the GMD Amplifier, the output is usually 10 volts in order to be compatible to the ADC full scale. Each individual system will have its own gain requirement per customer specification (see Section 5 for System Specifications)

- (a) Determine the input required to obtain a Full Scale reading on the ADC readout.
- (b) Introduce the input between the HI and LO input of the GMD multiplexer.
- (c) Adjust the gain potentiometer to obtain a full scale reading on the ADC output.

2.9.4 Check the ZERO and GAIN adjustments again and make the necessary adjustments.

MODEL GMD AMPLIFIER MULTIPLEXER (HIGH GAIN)

2.10 FUNCTIONAL DESCRIPTION MODEL GMD (Figure 2.1)

The Model GMD Amplifier Multiplexer High Gain Version is a Differential Input Amplifier followed by a single-ended input, single-ended output semiconductor switch.

Figure 2.5 is an over-all Block Diagram of the Model GMD Multiplexer in a system application. Analog signals are connected to the multiplexer channels by shielded cabling from the rear connector. Each multiplexer board contains, one amplifier, one multiplexer switch, associated drive control logic and analog overhead clamps.

Control of the multiplexer channels may be directed from the front panel (optional GMC Logic Control Package, see Section 3 and Figure 2.5) or by the customer interface at the rear panel connector (refer to Section 1).

2.11 SPECIFICATIONS

The specifications set forth in the following sections should be combined with the A/D Converter specification (refer to Page 8 of the GM Series A/D Conversion System brochure) in arriving at a total system performance specification.

2.11.1 Gain: One fixed gain between the range of 10 to 1000, customer specified.

2.11.2 Gain Accuracy: $\pm 0.01\%$

2.11.3 Gain stability (at constant temperature): $\pm 0.01\%$

2.11.4 Gain temperature coefficient: 20 ppm/ $^{\circ}\text{C}$

2.11.5 Linearity: $\pm 0.01\%$

- 2.11.6 Zero stability: 10 microvolts RTI and 1 millivolt RTO for 48 hours
- 2.11.7 Zero temperature coefficient: 1 microvolt/⁰C RTI and 0.1 millivolt/⁰C RTO
- 2.11.8 Input impedance: 10 megohms
- 2.11.9 Shunting capacitance: Selected for system requirements.*
*Depends on source impedance and data bandwidth requirements.
- 2.11.10 Common mode rejection: 60 db + gain or 108 db DC to 60 Hz (whichever is smaller)
- 2.11.11 Common mode voltage: 10 volts peak AC or DC for balanced inputs, 5 volts peak for single-ended inputs
- 2.11.12 Pumpout current: 10^{-8} amperes
- 2.11.13 Input connection: Three wires . . . Input high, input low and input guard
NOTE: The signal source must not be floating.
It may have no more than 10 megohms impedance to ground.
- 2.11.14 Normal Mode voltage: 20 volts maximum
- 2.11.15 Input overload recovery: Less than 1 millisecond to 0.01% FS ± 10 microvolts RTI at full bandwidth
- 2.11.16 Crosstalk: Less than 0.01% ± 3 microvolts RTI
- 2.11.17 Bandwidth: -3db at 20 kHz
- 2.11.18 Settling time: 100 microseconds to 0.01% ± 10 microvolts RTI
NOTE: Settling time increases as input bandwidth decreases.
- 2.11.19 Noise: Less than 20 microvolts peak RTI plus 1 millivolt peak RTO
- 2.11.20 Output (to ADC System): Commutated ± 10 volts full scale
- 2.11.21 Output impedance - ON: 500 ohms maximum
- 2.11.22 Output leakage current - OFF: 15 nanoamps maximum
- 2.11.23 Crosstalk: 0.01% of full scale maximum for 100 channels

- 2.11.24 Switching time: 1 microsecond to 0.01% of full scale into a load of 10 megohms shunted by 50 pf. (Analog buss should be guarded and driven externally if load capacity exceeds 50 pf or if insulation exhibits dielectric absorption)
- 2.11.25 Temperature: The amplifiers will meet the stated specifications over a temperature range of 0°C to +50°C.

2.12 OPERATING INSTRUCTIONS

The System Multiplexer may be totally controlled by the customer or may be controlled by the optional GMC Logic Control Package described in Section 3. A description of these control methods appear in Sections 1 and 3 of this manual.

2.13 THEORY (Figure 2.6)

The multiplexer switch is a FET (Field Effect Transistor). Figure 2.2 shows a schematic of the GMD Amplifier Multiplexer displaying the channel address circuit, amplifier, and the FET switch circuit. Because the FET has no inherent offset voltage, whatever signal appears on the input will also appear on the output (when the switch is ON). One characteristic of the FET used in the Model GMD is that the switch is normally ON with a ZERO gate voltage and is turned OFF by the application of a negative voltage of significant value applied to the gate.

Also shown in Figure 2.6, the output of the GMD Amplifier output is connected to the DRAIN (D) and the multiplexer output is connected to the SOURCE (S) of the FET. When the gate is released from its negative potential and assumes the potential of the DRAIN, the FET will

2.13 (continued)

turn ON and the SOURCE will be brought to the potential of the DRAIN.

The multiplexer switch and its input amplifier appear in Block Diagram form in Figure 2.7.

2.14 CALIBRATION

2.14.1 Common Mode adjustment

- (a) Tie the input HI and input LO together
- (b) Apply a 20 volt, 60 Hz, AC signal source between the tied-together inputs and ground.
- (c) Observe the testpoint marked AMP OUT. Adjust the CM potentiometer for minimum output (20 millivolt scale).

2.14.2 ZERO

Short the input of the multiplexer and adjust the ZERO potentiometer for a zero reading on the ADC readout (within the accuracy of the system).

2.14.3 GAIN

Regardless of the Gain of the GMD Amplifier, the output is usually 10 volts in order to be compatible to the ADC full scale. Each individual system will have its own gain requirement per customer specification (see Section 5 for System Specifications).

- (a) Determine the input required to obtain a Full Scale reading on the ADC readout.
- (b) Introduce that input between the HI and LO input of the GMD multiplexer.

2.14.3 (c) Adjust the gain potentiometer to obtain a full scale reading on the ADC output.

2.14.4 Check the ZERO and GAIN adjustments again and make the necessary adjustments.

SECTION 3
GMC LOGIC CONTROL SYSTEM
(Optional Multiplexer System Control)

3.1 INTRODUCTION

When the optional GMC Logic Control is included in the MUX/ADC combination, the system may be operated in many different modes. A basic introduction to the modes of operation appears in Section 1 of this manual.

The following series of paragraphs gives a functional description for the switches and controls located on the front panel.

- 3.1.1 FIRST ADDRESS: Selection of single channel address when MODE Switch is in RANDOM TEST, MAN or CONT: Selection of the first channel in a series when the MODE Switch is in NORMAL, SEQUENTIAL TEST, MAN or CONT.
- 3.1.2 LAST ADDRESS: Selection of the last channel when the MODE Switch is in NORMAL, SEQUENTIAL TEST, MAN or CONT.

3.1.3 MODE Switch

- (a) NORM (Normal . . . In this position, the primary control of the multiplexer is at the customer's command via the rear connectors.
- (b) RANDOM TEST . . . Relates to the FIRST MUX ADDRESS only. When the MODE Switch is on the RANDOM TEST-MAN position, depressing the MANUAL button will select the channel indicated by the FIRST MUX ADDRESS. When the MODE Switch is in the RANDOM TEST CONT position, the control will automatically and continuously select the channel indicated by the FIRST MUX ADDRESS.
- (c) SEQUENTIAL TEST . . . This psotion incorporates both FIRST MUX ADDRESS and LAST MUX ADDRESS switches. When the MODE Switch is in the SEQUENTIAL TEST-MAN position, depressing the manual button will select, in order, the channels between and including FIRST and LAST MUX ADDRESS. Turning the MODE Switch to the SEQUENTIAL TEST-CONT position will allow an internal clock to sequence through the channels between and including the channels indicated by the FIRST and LAST MUX ADDRESS switches.

3.1.4 Test Points . . . Monitoring points only for specified signals of interest. In the standard configuration, the following signals may be monitored from the front panel test points: EXAD, COIN, CLOCK, BUSY, GND, and TADC

3.2 INPUT CONTROL LINES (REAR PANEL CONNECTOR)

The following is a list of input control lines associated with the GMC Control System.

- 3.2.1 ADDRESS . . . This is a multiplexer channel binary address externally furnished to randomly select a particular multiplexer channel. A TTL compatible binary word of four or more bits in length is required. This address is only effective when the front panel GMC Control Package MODE Switch is in the NORMAL position.
- 3.2.2 CLOCK (CLK) . . . The CLOCK function is an externally furnished TTL pulse, 100 nanoseconds minimum width, which is used in conjunction with the (ADD-X, EXAD) function to (1) gate in the random binary address or (2) advance the multiplexer to the next channel. The CLOCK function also sets the proper delays to initiate the A/D Conversion process.
- 3.2.3 ADDRESS TRANSFER (ADD-X, EXAD) . . . The ADD-X function is a TTL level which established the mode of operation for the external CLOCK function. When the ADD-X level is true the CLOCK function will be used to gate in the random channel address from an external source i.e., computer . . . and when the level is false, the CLOCK function will be used to sequentially advance the multiplexer channels within the limits established by the front panel MUX Address switches. The ADD-X function is effective when the front panel GMC Control Package MODE Switch is in the NORMAL position.

When sequentially advancing to the channel selected by the LAST MUX ADDRESS switches, the next CLOCK pulse will cause the channel indicated by the FIRST MUX ADDRESS switches to be selected.

3.2.4 RESET . . . The RESET function is an externally furnished TTL level, used to reset the internal register to the channel selected by the front panel FIRST MUX ADDRESS switches. Application of the RESET and CLOCK function will initiate a return to the channel selected by the FIRST MUX ADDRESS switches. Reset does initiate a conversion of the first channel. When the RESET function is not being used, it should be tied to the digital ground.

3.3 OUTPUT CONTROL LINES

- 3.3.1 NORMAL MODE . . . The NORMAL MODE function relates to the position of the front panel MODE switches for either or both the ADC and the multiplexer. When both of these front panel switches are placed in the NORM position, the signal on the designated pin of the rear connector (see customer connection drawing in Section 8) will appear as a TTL level HI with reference to ground. If either switch is changed to another position, the signal at the rear connector will appear as a TTL level LO.
- 3.3.2 END of SCAN (COIN) . . . The COIN function is a TTL level which becomes "true" upon selecting the "last channel" for digitizing as established by the front panel address.
- 3.3.3 BUSY . . . Indicates that the system is BUSY. Refer to the Test Report for the specific timing.
- 3.3.4 EOC . . . The A/D Converter will also provide a separate EOC function as indication that the conversion is complete and the data lines have settled. This appears as a TTL pulse 100 nanoseconds minimum width. The EOC function may be used as an output data strobe.

SECTION 4

ANALOG-TO-DIGITAL CONVERTER

4.1 FUNCTION DESCRIPTION

The Model GM Series Analog-to-Digital Converter is a solid state device that will upon command produce a binary digital representation of an analog input signal.

The digital output of the ADC is presented in a parallel binary word. The output code is customer specified. For full scale, conversion speed, accuracy, and timing, refer to the Test Report in Section 10.

The speed of the conversion or throughput rate varies with the model and resolution of the converter. The inclusion of a Sample-and-Hold Amplifier and/or multiplexer channels also affects the total conversion time of the system. Refer to Section 5 of this manual for unique specifications concerning the entire system. Specifications located in this section are for the ADC only and do not represent the system operation.

4.2 SPECIFICATIONS

4.2.1 Conversion Rates

GMAD-1

14 binary bits and sign	750 kHz
13 binary bits and sign	760 kHz
12 binary bits and sign	800 kHz
11 binary bits and sign	1 MHz

4.2.2 Conversion Times

GMAD-1

14 binary bits and sign	1.5 microseconds
13 binary bits and sign	1.4 microseconds
12 binary bits and sign	1.2 microseconds
11 binary bits and sign	1 microsecond

4.2.3 Input Impedance: 100 megohms or greater

4.2.4 Source Impedance: 1000 ohms maximum

4.2.5 Data Outputs: TTL

4.2.6 Output Code

(a) BINARY

True bipolar

One's Complement

Two's Complement

(b) BCD

True bipolar

Nine's Complement

Ten's Complement

4.2.7 Accuracy

14 binary bits and sign	±0.01%	±1/2 LSB
13 binary bits and sign	±0.015%	±1/2 LSB
12 binary bits and sign	±0.025%	±1/2 LSB
11 binary bits and sign	±0.05%	±1/2 LSB
10 binary bits and sign	±0.1%	±1/2 LSB
9 binary bits and sign	±0.2%	±1/2 LSB

4.2.7 (continued)

8 binary bits and sign $\pm 0.4\%$ $\pm 1/2$ LSB

7 binary bits and sign $\pm 0.8\%$ $\pm 1/2$ LSB

4.2.8 Input Voltage Range

Standard ranges are from ± 5 volts to ± 10 volts. Other ranges are available upon special request.

4.2.9 Digitize Command

Positive or negative slope and pulse width greater than 10 nanoseconds.

4.2.10 End-of-Conversion

Parallel data ready indication; nominal pulse duration of 100 nanoseconds.

4.2.11 Power

The ADC Systems are equipped with their own integral DC power supply and require only standard line voltage (115v AC $\pm 10\%$, 60 Hz).

4.2.12 Sample-and-Hold GMSH-10 and GMSH-100

Gain: 1.000 $\pm 0.01\%$

Gain Stability and Linearity: $\pm 0.01\%$ of full scale

Input Impedance: Greater than 100 megohms.

Source Impedance: 0 to 1000 ohms.

Output Impedance: Less than 1 ohm.

Output Load: 200 ohms minimum, 500 pf maximum.

Settling Time (acquisition time to 0.01%) Sample Modes:

(a) GMSH-10

0.5 microseconds from one full scale polarity to the opposite polarity (10 volts full scale)

(b) GMSH-100

2 microseconds from one full scale polarity to the opposite polarity (10 volts full scale).

Hold Delay

(a) GMSH-10: 0.25 microseconds after HOLD pulse leading edge.

(b) GMSH-100: 1 microsecond after HOLD pulse leading edge.

4.2.12 (continued)

Hold Aperture

(a) GMSH-10: 10 nanoseconds

(b) GMSH-100: 50 nanoseconds

Noise: 0.5 millivolts peak

Droop in HOLD Mode: +1 millivolt after 1 millisecond.

4.2.13 Operating Temperature

The converter will perform to the specifications stated, within a temperature range of 0⁰ to +50⁰C.

4.2.14 Cooling

For proper operation, the air surrounding the converter should be maintained between 0⁰C and +50⁰C, with a relative humidity not to exceed 70%. The converter utilizes its own fan for internal cooling.

4.2.15 Storage Conditions

The converter will show no deterioration when subjected to storage temperatures of -55⁰C to +85⁰C and to relative humidities of up to 100% without condensation.

4.2.16 Size: The dimensions of the converter are 20 or 26-1/2 inches in length (total); 19 inches in width; and 5-1/4 inches in height.

4.2.17 Weight: The converter weighs 45 - 55 pounds (shipping weight is 60-75 pounds).

4.2.18 Mounting: The converter will mount into a standard 19-inch RETMA Rack.

4.3 OPERATING INSTRUCTIONS

The system operation of the GM Series ADC is covered in Section 1 and Section 3. Special system sequencing or operations may be found in Section 5 System Description.

4.3.1 ADC Front Panel Controls

Three controls related to the ADC in the system are located on the front panel. These are ADC Trigger Function Switch, ADC Trigger Pushbutton Switch, and ADC Zero.

The ADC Trigger function switch has three positions:

- (a) NORM (Normal) position: This position is used when the ADC is being triggered by the systems GMC Logic Control Package (See Sections 1 and 3).
- (b) INT (Internal): This position provides constant asynchronous conversion of the analog input at a rate determined by an internal clock located on the ADC timing circuit board (Clock frequency is typically 10 Hz).
- (c) MAN (Manual: Placing the function switch in this position will allow a new conversion to be initiated each time that the ADC pushbutton switch is depressed.

The ADC Zero is a recessed screwdriver adjustable potentiometer to allow for the correction of zero offsets that may be caused by peripheral equipment.

4.4 THEORY (Figure 4.1, 4.2, 4.3)

The GM series Analog-to-Digital Converter consists of a series of similar bit boards. Each bit board consists of two basic elements. These elements are: (1) an analog circuit for each individual bit and (2) a logic storage and decoding section for each individual bit (refer to Figure 4.1).

In the GM Analog-to-Digital Converter, several of the above described bit boards are connected in series as indicated in Figure 4.1, and each circuit receives, as its input, the output of the preceding circuit.

Each individual analog circuit is identical in operation. Schematically, the bit board (printed circuit) part values will change from the MSB to the LSB due to the decreased resolution of each successive bit board.

Using the block diagram in Figure 4.1, note that each bit board, including the sign, has its own analog circuit and logic storage. The buffer is used to provide a high impedance to the source.

Each converter stage has the same transfer function as indicated in Figure 4.2. If the "X" axis is the input signal of each of the analog circuits, then the "Y" axis in the resultant analog output of the circuit, e.g., as the input varies from minus 10 volts to plus 10 volts, the resultant output of the analog circuit will vary from plus 10 volts to minus 10 volts and back to plus 10 volts.

The logic storage stage is designed to give a logic output as follows: For all positive inputs to the analog circuit, the logic output will be a "0" and for all negative inputs, the logic output will be "1".

4.4 (continued)

Figure 4.3 shows the operation of a minus 10 volt to plus 10 volt signal and the subsequent outputs of each amplifier, along with the logic ("1" or "0"). For positive inputs, a logic "0" is realized and for negative inputs, a logic "1" is realized. In this manner, a Gray code logic may be obtained as a representative digital value of the input to the ADC.

The ADC operates in the Gray code rather than normal binary because this allows the progression of the code to advance only one bit at a time. To convert the Gray code into normal binary, the storage and decoding sections (see Figure 4.3) use the following process: Starting with the MSB, which is connected to give a binary output that is the complement of the Gray code, each time a bit board is preceded by data output that is a "1" logical, that bit is reversed ("0" to a "1" and vice-versa). See the binary and Gray codes in Figure 4.3 for an example.

The GM Analog-to-Digital Converter follows the input signal at all times. To receive a digital representation of the input at any time, all that is necessary is to gate the storage sections simultaneously. The logic is then converted from a Gray code to binary and released to the output.

4.5 BIT BOARD DESCRIPTION

Figure 4.4 is a block diagram of a bit board, the fundamental building block of the converter. The diagram includes the input amplifier (A1), the output amplifier (A2), the zero crossing detectors, the logic storage and decode logic.

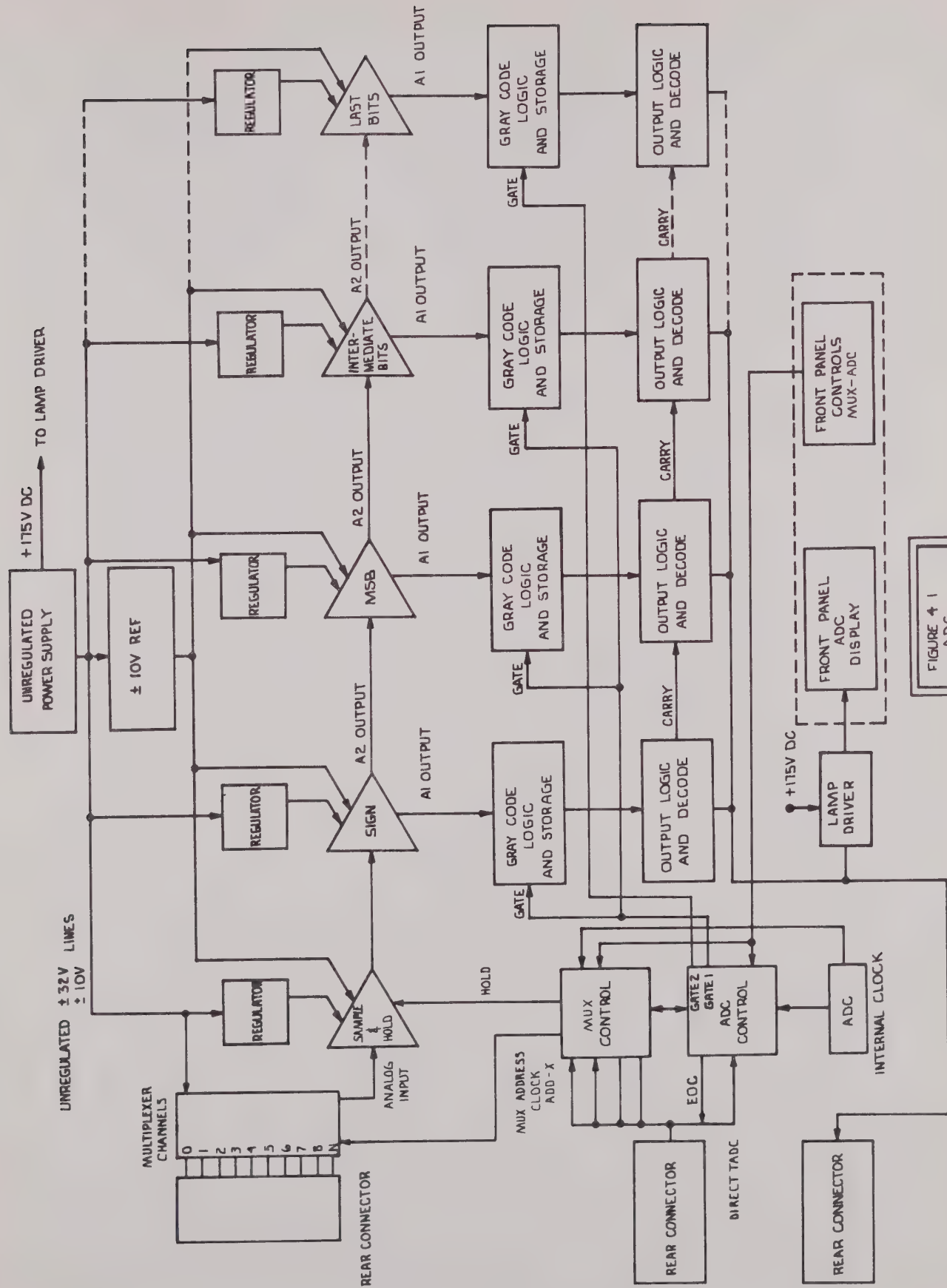


FIGURE 4-1
ADC
BLOCK DIAGRAM

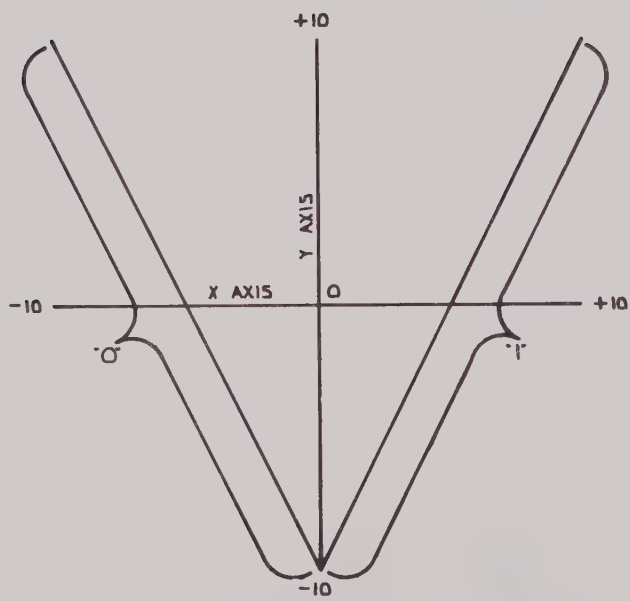


FIGURE 4.2

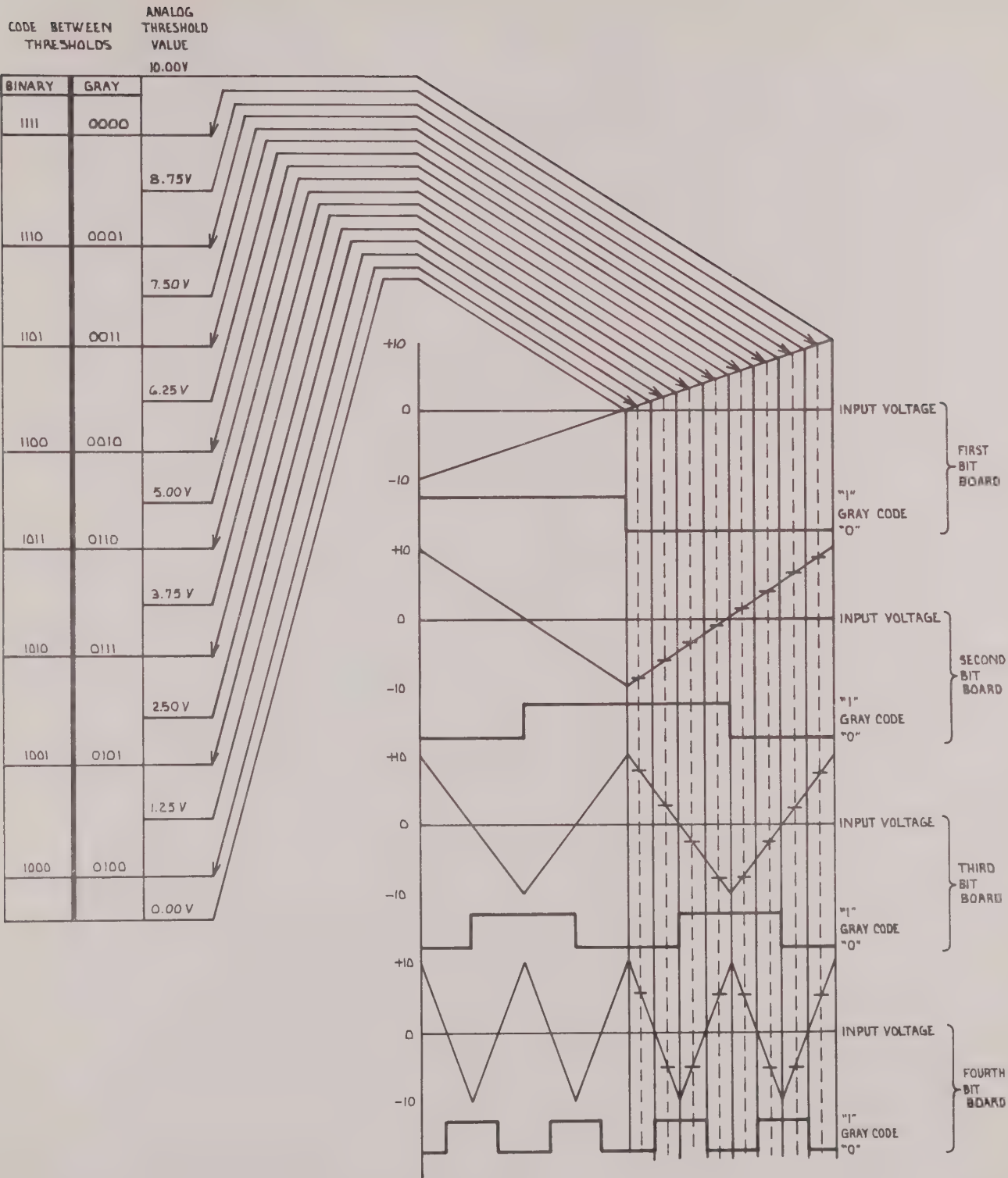


FIG. 4.3

4.5 (continued)

Amplifier A1 output is connected to the zero crossing detectors and, depending upon whether the input to the amplifier is negative or positive, sets the logic of IC A3. The logic of IC A3 is stored at IC A3 when the GATE pulse is received. When the GATE pulse is received (the GATE pulses are also named UPDATE ADC and may be observed at the control board on test points marked DELAY 1 and DELAY 2), the logic is transferred to the IC's A1 and A2. Through interconnection with the subsequent and preceding bit boards, the Gray code is converted into the correct binary output.

The output of Amplifier A2 is fed to the input of the next bit board and the above process is repeated.

In operation, when all of the bit board's logic is settled the GATE pulse is applied and the binary digital representation of the analog input appears at the output and is displayed on the front panel.

4.6 BUFFER OR SAMPLE-AND-HOLD

When the bandwidth of the analog input signal is below approximately 100 Hz a Buffer Amplifier is normally incorporated between the multiplexer output buss and the ADC. The buffer provides a high impedance load to the output of the multiplexer. The Buffer Amplifier is available in both differential and single-ended configurations. The gain of the buffer is dependent upon the full scale of the ADC.

When wide bandwidth data is encountered, a Model GMSH Sample-and-Hold Amplifier is employed.

Figure 4.5 is a block diagram of the GM Series Sample-and-Hold Amplifier. The basic design is two amplifiers in series. The first amplifier may be either differential or single-ended and provides a high input impedance with low output impedance for the Sample-and-Hold Amplifier.

The second amplifier is connected as an integrating amplifier. This amplifier follows the output of the first amplifier until the sample-and-hold command switches from the sample mode to the hold mode. When the command goes to "hold", the second amplifier is disconnected from the first amplifier and its own DC feedback and the signal that was last on the input of the integrating amplifier is held by the feedback capacitor. This DC signal can be held for as long as a millisecond before deterioration begins (see specifications Section 4.2)

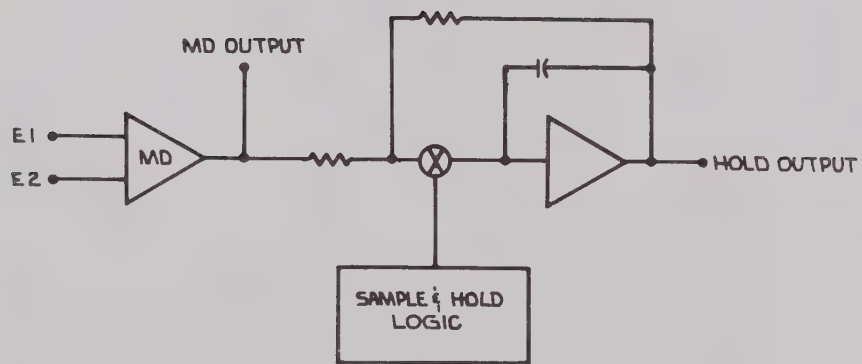


FIGURE 4.5

SECTION 5

SYSTEM DESCRIPTION

5.1 INTRODUCTION

This section contains a brief general outline of your particular system. It also contains information concerning special specifications or configurations of the system.

Your GM Series Analog-to-Digital Conversion System is described by the part number 58700. This part number describes a system consisting of: One channel Model GMD-100 Amplifier-Multiplexer (channel identification No. 1); two channels of Model GMD-1 Amplifier-Multiplexer (channel identification No's 2 and 3); wiring for a fourth Model GMD Series Amplifier Multiplexer (channel identification No. 0); 8 channels of Model GMM Multiplexer (channel identification No's 4 through 11); wiring for eight additional Model GMM Multiplexer channels (channel identification No's 12 through 19); a Model GMSH-100 Sample-and-Hold Amplifier incorporated between the multiplexer output buss and the input to the ADC; and a Model GMAD1-15B Analog-to-Digital Converter. Multiplexer channel selection may be random access binary address or sequential scan via the Model GMC Logic Control System. A Block Diagram of your system appears in Figure 5.1.

5.2 SPECIFICATIONS

Full Scale: Model GMD-1 Multiplexer: ± 10.24 volts
 Model GMD-100 Multiplexer: ± 0.1024 volts
 Model GMM Multiplexer: ± 10.24 volts
Resolution: 14 binary bits and sign
Output Code: Two's Complement

5.2 SPECIFICATIONS (continued)

Output Data: Both the true and false sides of the data will be available at the output connector.

Conversion time: 3.5 microseconds per channel

Logic: Positive True TTL.

5.3 SPECIAL FEATURE

Both the true and false sides of the sign line are made available at the rear connector. This function will allow the converter to be used as a "Zero crossing detector" in that the sign line will change as the input signal changes polarity. A control line will be provided to enable function.

When the above mode is used, the Sample-and-Hold Amplifier at the A/D input should remain in the "Sample" mode. (The multiplexer cannot be dynamically operated nor the SH/AD combination be commanded to convert when the "Zero crossing" mode is employed).

The System conforms to a Hughes Specification Number 258392 Rev. A.

The first and last channel of the multiplexer may be remotely addressed.

Also this system contains both low gain and high gain Model GMD Amplifier Multiplexers.

5.4 MULTIPLEXER EXPANSION MODULE

An expander module P/N 58845 that will increase the total channel capacity to 96 has been designed for use with the P/N 58700. This expander module consists of the following multiplexer models.

<u>MODEL</u>	<u>DESCRIPTION</u>	<u>CHANNEL NO.</u>
GMD-10	Full Scale ± 1.024 v	20 - 31
GMMD	Full Scale ± 10.24 v	32 - 71
GMD-0.5	Full Scale ± 20.48 v	72 - 79
GMD-0.25	Full Scale ± 40.96 v	80 - 91
GMD-0.125	Full Scale ± 81.92 v	92 - 95

Multiplexer channel control is via the Model GMC Logic Control Package mounted in the P/N 58700 Card Module.

5.4.1 Analog Outputs

The continuous analog output from the Model GMD channels 20, 21, 72, 73, 80, 81, 92, and 93 is available on one multiplin Winchester connector.

MULTIPLIED CHANNELS

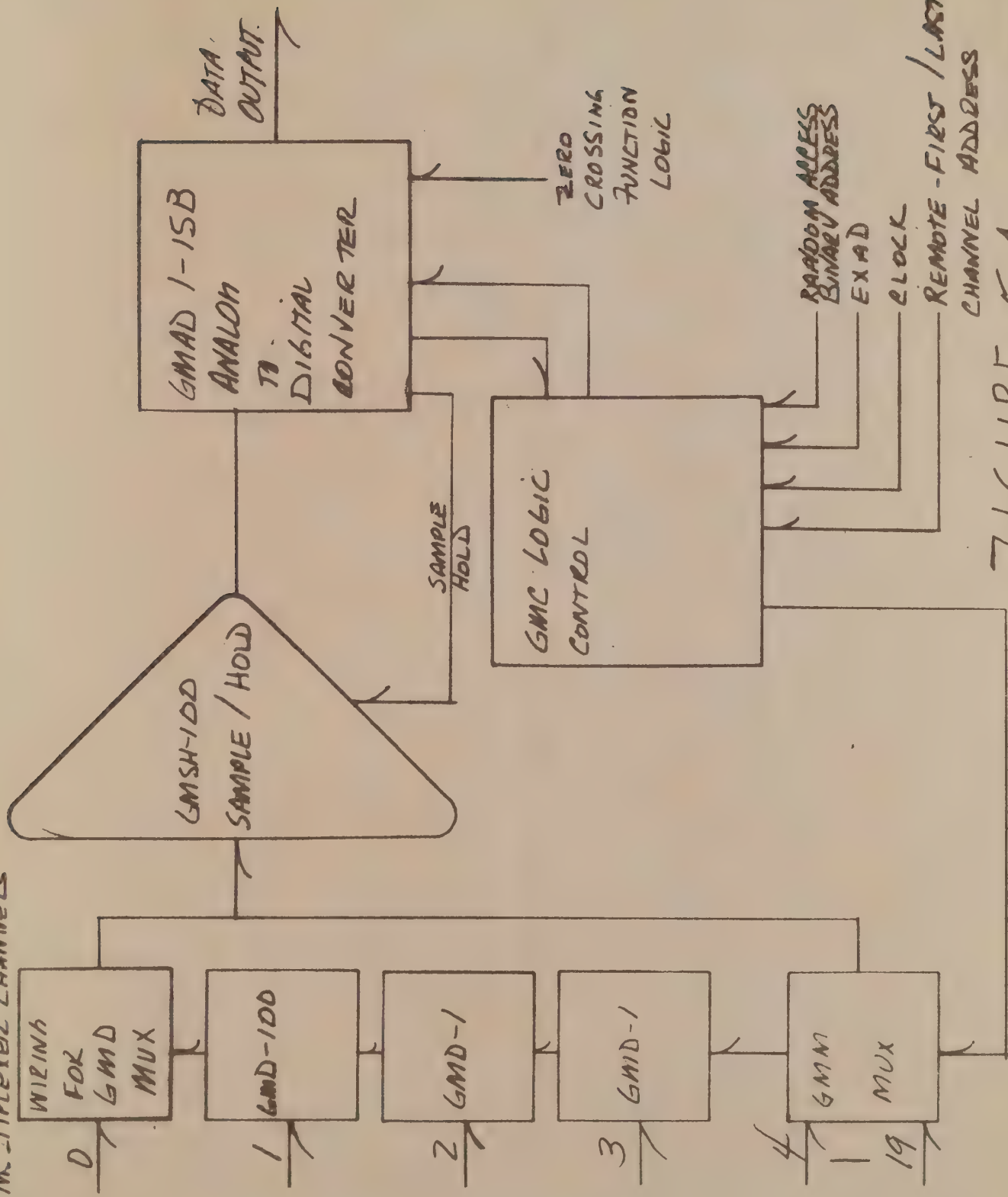


FIGURE 5.1

SELECT LINES

SVS-58100-4018

SECTION 6

CALIBRATION

6.1 INTRODUCTION

This calibration procedure describes the step-by-step method for calibrating the GM Series Multiplexing Analog-to-Digital Conversion System. Hardware and placement of certain boards may be different depending upon each customer's requirement, but basic calibration is the same for each individual instrument.

Please refer to the basic assembly for the individual plug-in board placement. Refer to the assembly drawings of each individual plug-in board for variable resistor and capacitor placement, pin numbers, and test points. All of the above are located in Section 8.

When making the adjustments in the preliminary and final calibration it will be necessary to maintain a proper air flow within the chassis. For the preliminary calibration remove the top cover, turn it over and place it on the top of the unit so that only the first row of boards will be visible. This will maintain the near proper air flow and still allow access to the ADC calibration and timing adjustment that will be made during the preliminary calibration.

During the final calibration, the unit will most likely be in an environmental chamber. The top and bottom covers should be in place during the measurements. If an adjustment is necessary, the cover can be removed for these adjustments. However, it is recommended that the adjustment be made in the shortest time possible and the cover be replaced after the adjustment has been made. After the cover has been replaced, time should be allowed for the air flow to return to normal before recording any further measurements.

6.2 TEST EQUIPMENT

Equipment recommended for calibration consists of the following:

- (a) A stable DC analog voltage source, variable over the range of $\pm$ full scale input voltage or ± 10 volts whichever is greater. The voltage resolution should be at least 25% of the least significant bit. The source impedance should be less than 1000 ohms.
- (b) Oscilloscope, Tektronix 545A, with 1A5 and CA Preamplifiers, or equivalent.
- (c) Five-digit digital voltmeter, differential voltmeter, or equivalent. The accuracy should be at least twice that of the system being tested.
- (d) Triangle wave generator with a capability of 20 volts peak-to-peak into a 470 ohm load at 1 kHz.
- (e) Volt ohmeter such as Simpson 260.
- (f) Pulse generator to provide clock pulses of an equivalent in amplitude width and frequency to the normal system operating pulses.
- (g) Printed circuit card extender, bit board extender (Part No. 52315) and Sample-and-Hold Buffer extender (Part No. 52318). All three are supplied with the unit. (Part No. 52315 and 52318 may be replaced by a single extender Part No. 52330.)

6.3 PRELIMINARY CALIBRATION (at room temperature $25 \pm 3^\circ\text{C}$)

In the GM Series ADC each binary bit is controlled by a single printed circuit board with the exception of the four least significant bits. During calibration, each board will be adjusted individually starting with the least significant bit (excluding 1, 2, 4 and 8). There are some adjustments that relate to the least four bits and the adjustments are discussed in Section 6.3.3.

6.3.1 ADC (Figure 6.1)

- (a) Check the plus and minus reference supplies and set them for 10,000 volts.
- (b) Locate the least significant bit board (excluding the least four bits 1, 2, 4, and 8). This will be the AMP/Logic board nearest to 4 bit amplifier board. (Normally bits 1, 2, 4, and 8 are on two boards and are not adjusted per this procedure (See Section 6.3.3). If the ADC does not contain a four bit amplifier and a four bit logic board disregard Section 6.3.3 and begin the procedure with the least significant bit board.
- (c) Remove the next more significant AMP/Logic Board located just prior to the one mentioned in Step 6.3.1 (b) and replace it with the Bit Board Extender.
- (d) This board is designed to allow the operator to isolate a particular board from the higher order bits and introduce an input directly into that bit board. The operator may use a standard extender board and use the following pin numbers for connecting the input signal.

BIT BOARD EXTENDER	LABEL
Pin #9	Input Hi
Pin #4 and #5	Ground (low)

NOTE: JUMPER PINS 38 to 35 (logic).

For extender replacement of the Sample-and-Hold board, the pin numbers are as follows:

SAMPLE-AND-HOLD EXTENDER	LABEL
Pin #22	Input Hi
Pin #16	Input Low (Gnd.)

NOTE: DO NOT JUMPER PIN 38 to 35 AS ABOVE



6.3.1 (continued)

- (e) Connect the DVM through a 470 ohm resistor to the test points marked A2 and ANA GRD (Figure 6.1) located on the least significant bit board, (excluding the 4 bit amp and logic boards). This is normally the last "C" board. Connect the variable DC source with monitor) to the signal board extender (Pins 4 and 9). The input value must be measured directly at Pins 4 and 9 or remote sense lines must be used to compensate for the voltage drop in the input cable.
- (f) Set the DC source for minus 10 millivolts and note the reading of the DVM.
- (g) Set the variable DC source for plus 10 millivolts and adjust potentiometer label B0 so that a plus 10 millivolt input produces the same reading (at A2) as minus 10 millivolts did. Switch between plus 10 millivolts and minus 10 millivolts and adjust B0 with the plus 10 millivolts input until there is no change in the reading of the DVM.
- (h) Set the variable DC source for 0 VDC and adjust the potentiometer labeled zero until the reading at A2 is as close as possible to minus 10 volts.
- (i) Set the variable DC source for plus 10 volts and adjust potentiometer S2 for a plus 10,000 volt reading at test point A2 (Figure 6.1).
- (j) Set the variable DC source for minus 10 volts and adjust potentiometer S1 for a plus 10,000 volt reading at test point A2 (Fig. 6.1).
- (k) Repeat paragraph number two of step 6.3.1 (f) and (g) to check the symmetry.

6.3.1 (continued)

- (l) Repeat step 6.3.1 (h) to check the zero setting.
- (m) Repeat step 6.3.1 (i) and (j) to check the full scale of the bit board.
- (n) Return voltage input to 0 volts

6.3.2 Subsequent Bit Board Adjustment

- (a) Remove the signal board extender
- (b) Replace the bit board that had been previously removed.
- (c) Remove the next more significant bit board and insert the signal board extender.
- (d) Repeat steps 6.3.1 (f) through 6.3.1 (n) using the adjustment potentiometers on the first bit board after the extender board.

NOTE: When step 6.3.1 check is repeated, the reading on test point A2 on the last C board will be plus 10 volts.

- (e) Repeat 6.3.2 (a) through 6.3.2 (d) for all bit boards in sequence moving from the least to the most significant bit boards.

6.3.3 Four Bit Calibration (Figure 6.2)

- (a) Remove the bit board preceding the 4 bit amp.
- (b) Place the board extender into the slot
- (c) Connect a triangular wave generator to the signal board extender inputs.
- (d) Set the output of the generator for triangular wave of 20.0 volts peak-to-peak 1 kHz (symmetrical about zero + 10.0 to -10.0)
- (e) View the output AMP 1 on an oscilloscope and set the symmetry B0 1 so that all waves on the scope are symmetrical about the triangle peaks.
- (f) Set the potentiometer Z1 so that the output is symmetrical about zero.
- (g) Repeat steps 6.3.3 (e) and (f) for amplifier output AMP 2 using B02 and Z2 potentiometers.
- (h) View the test point for AMP 3 and adjust B0 3 and B0 4 so that there is less than 10% phase modulation of the displayed square wave over one cycle of sawtooth wave.
- (i) Remove triangle waveform and replace it with a DC source variable -10v to +10v. Remote sense not required.
- (j) Adjust voltage source as required to produce all digital counts on least significant bits per 4 bit amp linearity sheet (Figure 6.1.1) Note voltages. Remove DC source.
- (k) If the voltages are not within ± 0.2 volts of the listed values, reconnect the triangular wave form per 6.3.3 (c) and repeat 6.3.3 (d) through 6.3.3 (i).



FRONT PANEL INDICATORS 8, 4, 2, 1		THEORETICAL INPUT (VOLTS)	ACTUAL INPUT (VOLTS)	ERROR
0000	0001	+8.75		
0001	0010	+7.5		
0010	0011	+6.25		
0011	0100	+5		
0100	0101	+3.75		
0101	0110	+2.5		
0110	0111	+1.25		
0111	1000	0		
1000	1001	-1.25		
1001	1010	-2.5		
1010	1011	-3.75		
1011	1100	-5		
1100	1101	-6.25		
1101	1110	-7.5		
1110	1111	-8.75		

4 BIT AMP LINEARITY

Indicates Transition between
two given codes

FIGURE 6.1.1

6.4 BUFFER AMPLIFIER

6.4.1 Preliminary

All GM Analog-to-Digital Converters will have either a Sample-and-Hold or a Buffer Amplifier at the input to the ADC.

The calibration of the Buffer Amplifier should be done after the calibration of the ADC bit boards in order to allow the ADC to be used as a measuring instrument.

If there is not a multiplexer involved in the same chassis as the ADC, direct connection to the input of the buffer can be accomplished at the rear panel connector.

If a multiplexer is involved in the ADC chassis, connection to the input of the buffer may be accomplished by either of two methods:

- (a) Selection and addressing of a particular multiplexer channel and removal of the board containing that channel to enable connection to the input of the buffer through the common buss line of the multiplexer using the extender board.
- (b) Selection and addressing of a particular multiplexer channel and removal of the board containing that channel and then placing the Buffer Amplifier on an extender board and connecting to the input of the buffer directly through the pins of the Buffer Amplifier itself.

6.4.2 Common Mode RTO (Refer to Figure 6.3)

The common mode adjustment need only be made if the Buffer Amplifier is to be used as a differential input device.

- (a) Tie the input HI and LO together.



6.4.2 (continued)

- (b) Apply a 5v, 60 Hz, ADC signal between the tied-together HI, LO and ground.
- (c) Observe the output at the test point marked OUTPUT and adjust the RTOCM potentiometer for a minimum output.
- (d) When a Common Mode RTO adjustment potentiometer appears on a Buffer Amplifier and the buffer is used as a single-ended input device, the CM RTO potentiometer is to be set to the center of its span.

6.4.3 ZERO (Refer to Figure 6.3)

Short E1 (input HI) to ground Monitor. The output at the test point between the RTO CM and GAIN potentiometers with a DVM and adjust the ZERO potentiometer for a 0.000 output.

6.4.4 GAIN (Refer to Figure 6.3)

The gain of the Buffer Amplifier in the GM ADC will depend upon the customer's input full scale and output code requirements.

Regardless of the buffer input characteristics the GM ADC operates on a 20 volt signal swing (+10 to -10 volts). Therefore, the gain of the buffer is adjusted to compensate for the input full scale requirements.

Also due to special requirement of the customer or the A/D System, the buffer may be non-inverting or inverting. The methods for calibration of the gain will vary depending on these amplifying characteristics of the buffer.

- (a) Non-Inverting: A gain of 1 buffer with a non-inverting output is calibrated by looking at the input and output differentially on an oscilloscope. Adjust the GAIN potentiometer until there

6.4.4 (continued)

(a) (continued)

is minimum difference between the input and output of the buffer.

NOTE 1. When the non-inverting buffer gain is other than a gain of 1, it will be necessary to use a divider on the input as in Figure 6.3.1.

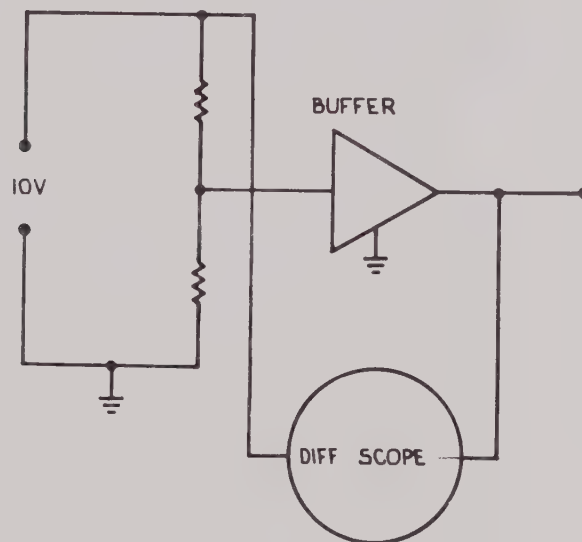


FIGURE 6.3.1

The input divider is selected to give an input to the buffer that will produce a full scale output. Measure the input against the output differentially on an oscilloscope and adjust the GAIN potentiometer for a null on the scope.

6.4.4 (continued)

- (b) Inverting: A gain of 1 buffer with an inverting output is calibrated by connecting the input and output per Figure 6.3.2.

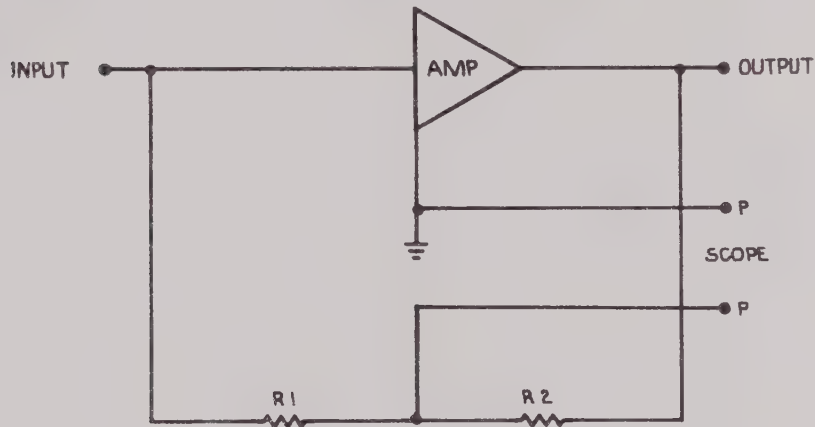


FIGURE 6.3.2

R1 and R2 are of equal value. Observe the output at test points P-P and adjust the gain for a minimum difference as indicated by the oscilloscope.

NOTE 2. When the inverting buffer gain is other than 1 it will be necessary to raise or lower the values of either R1 or R2 to compensate for the gain.

(c) Inverting or Non-Inverting (Alternate Method)

Introduce into the input of the buffer a value which will give a 10 volt output. This value is determined by the gain buffer which in turn is determined by the Full Scale of the ADC.

6.4.4 (c) (continued)

EXAMPLE: If the full scale of the ADC is 5 volts, the gain of the buffer will be two (2) to allow the ADC to operate at a 10 volt level. Adjust the GAIN potentiometer to bring the output of the buffer to ± 10 volts.

6.4.5 Total Systems Adjustments

With the assumption that the ADC has been calibrated separately per the procedure in Section 6, it will still be necessary to check calibration of the combination ADC-Buffer, ADC-Buffer-MUX, or ADC-S&H-MUX Assembly.

- (a) Set or verify that the front panel zero potentiometer is in approximately the center of its mechanical span.
- (b) Apply a zero input to the buffer through the rear connector. If a multiplexer is included select a single channel. If the multiplexer has an amplifier (Model GMD) in its circuitry, it will have to be calibrated separately before marking these system adjustments. Adjust the buffer zero potentiometer to produce a zero output in the digital output of the ADC System.
- (c) Using a near full scale input, adjust the GAIN potentiometer of the buffer to produce an equivalent digital output.

NOTE: The above statement are intended to be touch-up adjustments to the system and are only valid if the ADC has been previously calibrated as an individual part.

6.5 GMSH - SAMPLE-AND-HOLD AMPLIFIER (Optional) (Figure 6.4)

6.5.1 Preliminary

The calibration of the Sample-and-Hold Amplifier should be done after calibration of the Analog-to-Digital Converter. This allows the ADC in the system to be used as a measuring instrument. With reference to the inputs to the Sample-and-Hold, these inputs may be at the rear connector of the unit. However, if the Sample-and-Hold is between the multiplexer and the ADC, it will be necessary to select a multiplexer channel and use that channel for the input. Connect to the multiplexer channel either at the rear connector or remove the channel circuit board and introduce the signal at the common multiplexer output buss.

6.5.2 Common Mode

The Common Mode adjustment is necessary for all differential input Sample-and-Hold Amplifiers. Sample-and-Hold Amplifiers with single-ended inputs do not require a Common Mode adjustment; all that is necessary is that the Common Mode Potentiometer (RTCOM) be placed in the center of its span.

- (a) Tie the input HI and LO together
- (b) Apply a 5 vac 60 Hz sine wave between the combined HI-LO and ground.
- (c) Operate the system so that the unit is in sample or cycling between Sample-and-Hold.
- (d) Observe the output at the test point labeled "SH".
- (e) Adjust the RTCOM potentiometer for a minimum output.

FIGURE 6.4

6.5.3 Jump Adjustment (Figures 6.5, 6.6)

- (a) Verify that the ADC timing is correct and the ADC is running at or near the maximum rate.
- (b) Adjust the input to 0 volts.
- (c) View the output on the test point "SH" with an oscilloscope and adjust the JUMP potentiometer until both the Sample-and-Hold levels are settled to the same value as pictured in Figure 6.6.

NOTE: The above is done best with a sensitive oscilloscope preamp like the 1A5 or the scope input may be placed with the first A Board at the test point marked A2.

6.5.4 Preliminary Zero and Gain Settings

(a) Zero

Set the front panel zero potentiometer to the center of its span. Short the HI and LO together. Using an oscilloscope adjust the zero potentiometer for a zero output at the "SH" test point on the circuit card. This measurement should be made during the Hold period.

(b) Gain

Introduce a plus full scale signal (the amplifier may have gain) into the amplifier. Observe the test point "SH" with a DVM and adjust for a 10 volt output.

6.5.5 Final Jump Settings

Repeat steps 6.5.4 (a), (b) and (c).

6.5.6 Final Zero and Gain Settings

Repeat steps 6.5.3 (a) and (b)

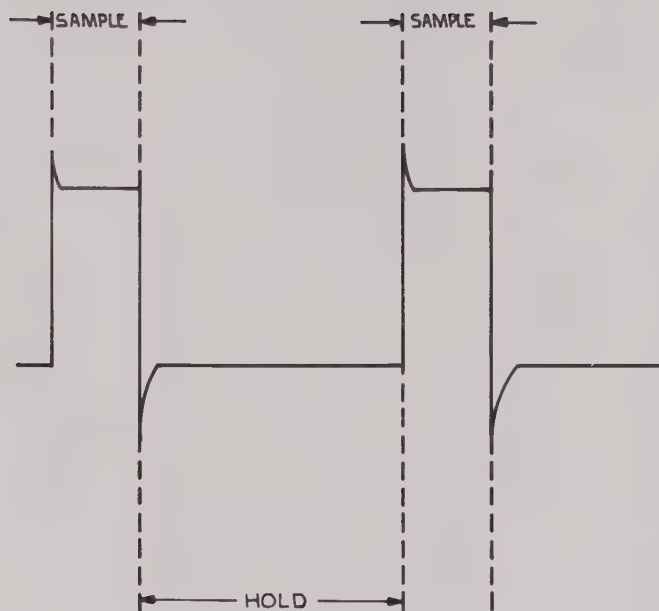


FIGURE 6.5

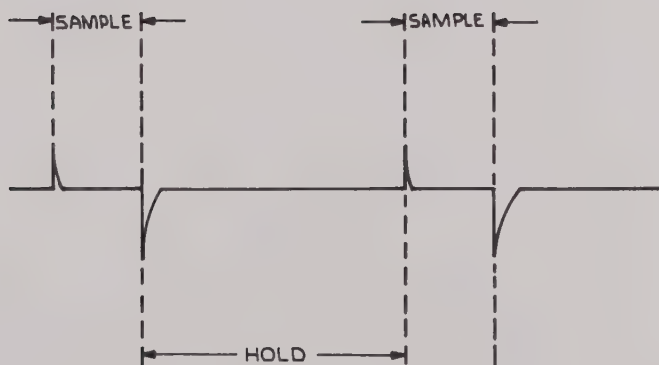


FIGURE 6.6

6.6 FINAL CALIBRATION

After the preliminary calibration has been completed, the major transition bit widths, linearity and over-all accuracy still must be verified.

6.6.1 Output Code

The output codes in this final check assume a Two's Complement output code. If the ADC is true bi-polar, it can easily and temporarily be converted to Two's Complement by removing the bottom cover and making the following changes:

- (a) Locate the wire that runs from the second "A" board MSB pin 33 to ground. Remove the end of the wire in pin 33 and connect it to the first "A" board (pin 32).
- (b) Connect a jumper from the first "A" board pin 35 to the second "A" board pin 36.

After completion of these final calibrations, the wires may be returned to their correct locations.

A One's Complement output code may be checked as if it were a Two's Complement and after making the required adjustments, the width of the combined + and - zero's are adjusted to be one bit wide. No actual logic exists to remove the extra zero code (- 11 111 111 111 111).

All examples shown are for a 14 bit and sign resolution. The same adjustments apply to lesser resolutions (down to 10 bits).

6.6.2 Initial Set-Up (Figures 6.7, 6.8)

- (a) With the rear panel power switch in the OFF position make all the necessary input and output connections. This includes control lines for the multiplexer (if present) AC power, analog inputs and external clock signal. If multiplexer inputs are present, connect them in groups per Figure 6.7 or 6.8.

NOTE: The analog inputs must never be left open

External control lines unless otherwise specified are standard TTL levels. Pulse widths are 100 nanoseconds minimum. Unused digital input control lines (reset, etc.) must be tied to digital ground.

- (b) Connect a voltage calibrator or a variable DC source with DVM to the analog input(s) and adjust the output of the calibrator for zero volts.
- (c) Place the power switch (rear panel) to the ON position and allow an one-half hour warm-up.
- (d) Adjust an external clock pulse generator to the maximum conversion rate of the ADC or system.
- (e) Using an oscilloscope, recheck the timing pulses for the correct settings (see Section 10 for the Test Report).
- (f) Check the plus and minus 10 volt reference supply.
- (g) Set the multiplexer channel to "0" if applicable.
- (h) Verify that the front-panel indicators are operating by varying the analog input.
- (i) Place the calibration (see the note on covers in the Introduction of Section 6) on the ADC and allow the airflow to stabilize for 5 minutes minimum.

These covers are especially made at our plant and have slots

6.6.2(i) (continued)

machined in them to permit access to the adjustment potentiometers. If one of these covers is used, one must still cover all of the remaining slots that are not being utilized for adjustments. If no special cover is available, adjustment may be made by removing the cover only for the adjustment. When this method is used, time should be permitted for the air flow to normalize after the cover has been replaced.

6.6.3 Sixteen (16) Point Linearity

The method used to determine corrections required is to plot a 16 pt linearity curve and compare it with the theoretical curve. Points plotted are at 1/4 scale increments from minus full scale to plus full scale. Actual transitions are plotted on both sides of major bits and near full scale. These points provide a picture of which adjustments are required for final calibration. This proves to be especially true when the actual bit is missing due to misadjustment.

Known D.C. voltages are applied to produce codes listed in Table 1. All codes are 1/8 scale increments are not normally plotted unless a problem condition is present. Only the $\pm 7/8$ scale transition points are plotted to verify that transition width. This also allows a better drift setting of the 4th A board zero at temperature. The specific points on Table 1 were selected to provide an easily recognized binary pattern.

Voltages required to produce these patterns are recorded and compared to the theoretical values. The algebraic differences, in millivolts, are plotted as errors on a vertical axis (See Figure 6.9). The horizontal axis show analog inputs from minus to plus full scale.

FRONT PANEL INDICATORS

(14 Bit & Sign) Two's Complement

ADC

TABLE I

Sign	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	THEORETICAL ANALOG INPUT (% f/s)	CORRESPONDING DC VOLTAGE (Volts) +10v f/s	
-	0	0	0	0	0	0	0	0	0	1	0	-----	*	-f/s	+19.5 cts	-9.9881	1
-	0	0	0	1	1	1	1	1	1	1	0		*	-7/8	-12.5 "	-8.7576	
-	0	0	1	0	0	0	0	0	0	1	0		*	-7/8	+19.5 "	-8.7381	
-	0	0	1	1	1	1	1	1	1	1	0		*	-3/4	-12.5 "	-7.5076	2
-	0	1	0	0	0	0	0	0	0	1	0		*	-3/4	+19.5 "	-7.4881	3
-	0	1	0	1	1	1	1	1	1	1	0		*	-5/8	-12.5 "	-6.2576	
-	0	1	1	0	0	0	0	0	0	1	0		*	-5/8	+19.5 "	-6.2381	
-	0	1	1	1	1	1	1	1	1	1	0		*	-1/2	-12.5 "	-5.0076	4
-	1	0	0	0	0	0	0	0	0	1	0		*	-1/2	+19.5 "	-4.9881	5
-	1	0	1	0	0	0	0	0	0	1	0		*	-3/8	-12.5 "	-3.7576	
-	1	0	1	0	0	0	0	0	0	1	0		*	-3/8	+19.5 "	-3.7381	
-	1	0	1	1	1	1	1	1	1	1	0		*	-1/4	-12.5 "	-2.5076	6
-	1	1	0	0	0	0	0	0	0	1	0		*	-1/4	+19.5 "	-2.4881	7
-	1	1	0	1	1	1	1	1	1	1	0		*	-1/8	-12.5 "	-1.2576	
-	1	1	1	0	0	0	0	0	0	1	0		*	-1/8	+19.5 "	-1.2381	
-	1	1	1	1	1	1	1	1	1	1	0		*	0	-12.5 "	- .0076	8
+	1	0	0	0	0	0	0	0	0	1	0		*	0	+19.5 "	+ .0119	9
+	0	0	0	1	1	1	1	1	1	1	0		*	+1/8	-12.5 "	+1.2424	
+	0	0	1	0	0	0	0	0	0	1	0		*	+1/8	-19.5 "	+1.2519	
+	0	0	1	1	1	1	1	1	1	1	0		*	+1/4	-12.5 "	+2.4924	10
+	0	1	0	0	0	0	0	0	0	1	0		*	+1/4	+19.5 "	+2.5119	11
+	0	1	0	1	1	1	1	1	1	1	0		*	+3/8	-12.5 "	+3.7424	
+	0	1	1	0	0	0	0	0	0	1	0		*	+3/8	+19.5 "	+3.7519	
+	0	1	1	1	1	1	1	1	1	1	0		*	+1/2	-12.5 "	+4.9924	12
+	1	0	0	0	0	0	0	0	0	1	0		*	+1/2	+19.5 "	+5.0119	13
+	1	0	0	1	1	1	1	1	1	1	0		*	+5/8	-12.5 "	+6.2424	
+	1	0	1	0	0	0	0	0	0	1	0		*	+5/8	+19.5 "	+6.2519	
+	1	0	1	1	1	1	1	1	1	1	0		*	+3/4	-12.5 "	+7.4924	14
+	1	1	0	0	0	0	0	0	0	1	0		*	+3/4	-19.5 "	+7.5119	15
+	1	1	0	1	1	1	1	1	1	1	0		*	+7/8	-12.5 "	+8.7424	
+	1	1	1	0	0	0	0	0	0	1	0		*	+7/8	+19.5 "	+8.7519	
+	1	1	1	1	1	1	1	1	1	1	0	-----	*	+f/s	-12.5 cts	+9.9924	16

$$1 \text{ Count} = \frac{f/s}{2^N} \quad \text{for } 10v, 14 \text{ bits}$$

$$= \frac{10}{2^{14}} = \frac{10}{16,384} \quad .61mv \quad 12.5 \text{ cts} = \frac{76 \text{ mv}}{19.5 \text{ cts} = 119 \text{ mv}}$$

$$= \frac{f/s}{2^N}$$

*The 3 least significant bits are used for the transition point recognition. The transition point is the point where the 3 to 4 binary change takes place. The lights will appear to be only partially ON and this should not be confused with the binary number 7 where all 3 indicators are ON full.

6.6.3

(continued)

Points are plotted from minus to plus full scale in sequence per Table 2. Points on each side of a transition point are plotted as though they occurred at the transition point. This means that transitions on both sides of a bit are plotted at the same horizontal coordinates.

Example: -2.5080 & -2.4877 (typical values) are plotted at -2.5v.

The important part is to connect points in proper sequence.

If all inputs corresponded exactly to the theoretical ones, a straight line with 0 errors like Figure 6.9(b) would result. With the transitions at zero width, any change due to drift or component aging could result in a reversal or "flipped" transition. This in turn could result in a missing bit. To avoid this the transition width is purposely adjusted to a width of approximately .8mv. Figure 6.9(a) shows all widths at .8mv.

The transition errors plotted on both sides of any bit must always be in a minus to plus direction. If not a correction must be made. When making corrections always make adjustments to least significant bits first since they affect more significant ones. Example: If 1st, 2nd, and 3rd "A" board adjustments are required, adjust 3rd "A" 1st, then 2nd, then 1st. It is normally a good practice to plot a curve after each adjustment to be sure only the intended changes were made and no others.

TABLE 2

Example: The curve of Figure 6.9(a) was plotted as follows:

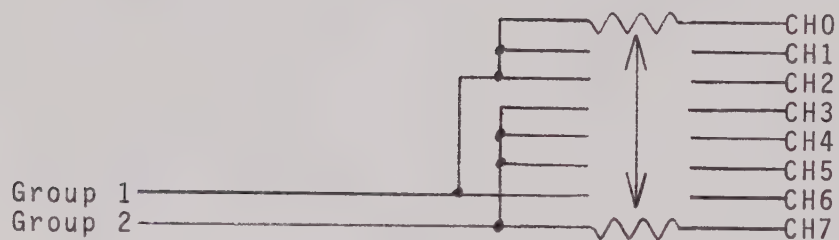
POINT	ACTUAL READING	THEORETICAL INPUT	ERROR (MV)	PLOT AT	
1	-9.9877	-9.9881	+.4	-10	-f/s
2	-7.5080	-7.5076	-.4	- 7.5	-3/4
3	-7.4877	-7.4881	+.4	- 7.5	-3/4
4	-5.0080	-5.0076	-.4	- 5	-1/2
5	-4.9877	-4.9881	+.4	- 5	-1/2
6	-2.5080	-2.5076	-.4	- 2.5	-1/4
7	-2.4877	-2.4881	+.4	- 2.5	-1/4
8	- .0080	- .0076	-.4	0	0
9	+ .0123	+ .0119	+.4	0	0
10	+2.4920	+2.4924	-.4	+ 2.5	+1/4
11	+2.5123	+2.5119	+.4	+ 2.5	+1/4
12	+4.9920	+4.9924	-.4	+ 5	+1/2
13	+5.0123	+5.0119	+.4	+ 5	+1/2
14	+7.4920	+7.4924	-.4	+ 7.5	+3/4
15	+7.5123	+7.5119	+.4	+ 7.5	+3/4
16	+9.9920	+9.9924	-.4	+10	+f/s

Numbers in example are for $\pm 10\text{v}$ inputs. With other full scale values the numbers would be different but proportional.

SINGLE-ENDED INPUTS

FIGURE 6.7

ALL RESISTORS 1000 Ω

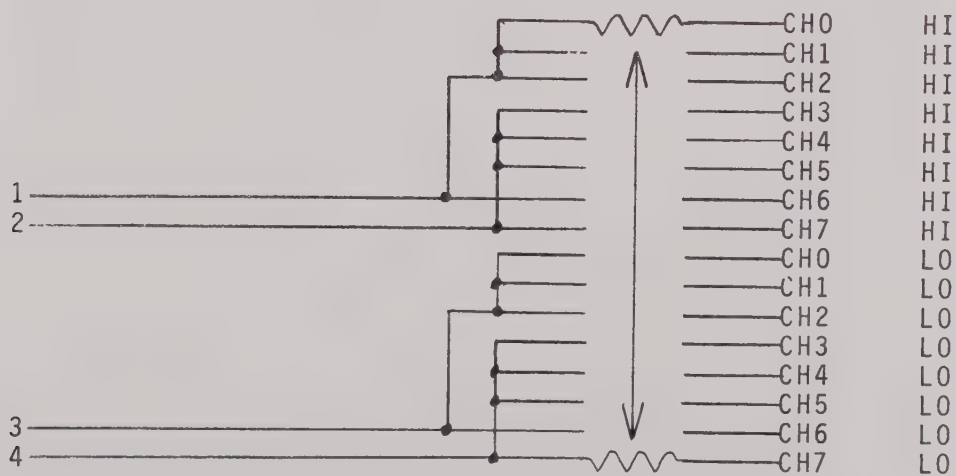


Lo inputs tied to analog gnd. If more channels are present than 8 this same pattern is repeated.

DIFFERENTIAL INPUTS

FIGURE 6.8

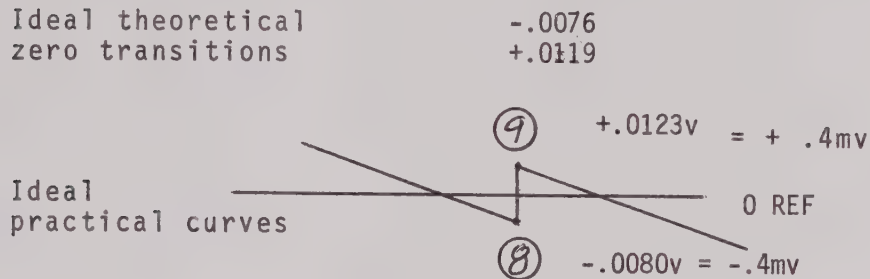
ALL RESISTORS 1000 Ω



6.6.3 (continued)

In Figure 6.9(a) all errors are .4mv in the correct directions.

Example from Figure 6.9(a):



Slopes of the segments should all be similar. If the slopes are not similar, certain adjustments may be made to correct the slopes (see S1 and S2 adjustment curves).

Observe symmetry of adjustments in curves in Figures 6-11 through 6-22.

The four important items displayed on these curves are:

1. Transition widths
2. Slopes
3. Zero Offsets
4. Gain Errors

For this reason, no attempt is made to correct it to the ideal theoretical curve (Figure 6.9(b)). The curve instead, is corrected to one similar to Figure 6.9(a), the ideal practical curve. Real curves do not usually look as perfectly symmetrical as the curve in Figure 6.9(a), however, all points must be within the over-all accuracy of the ADC under test.

ERROR
(MV)

+2
+1
0
-1
-2

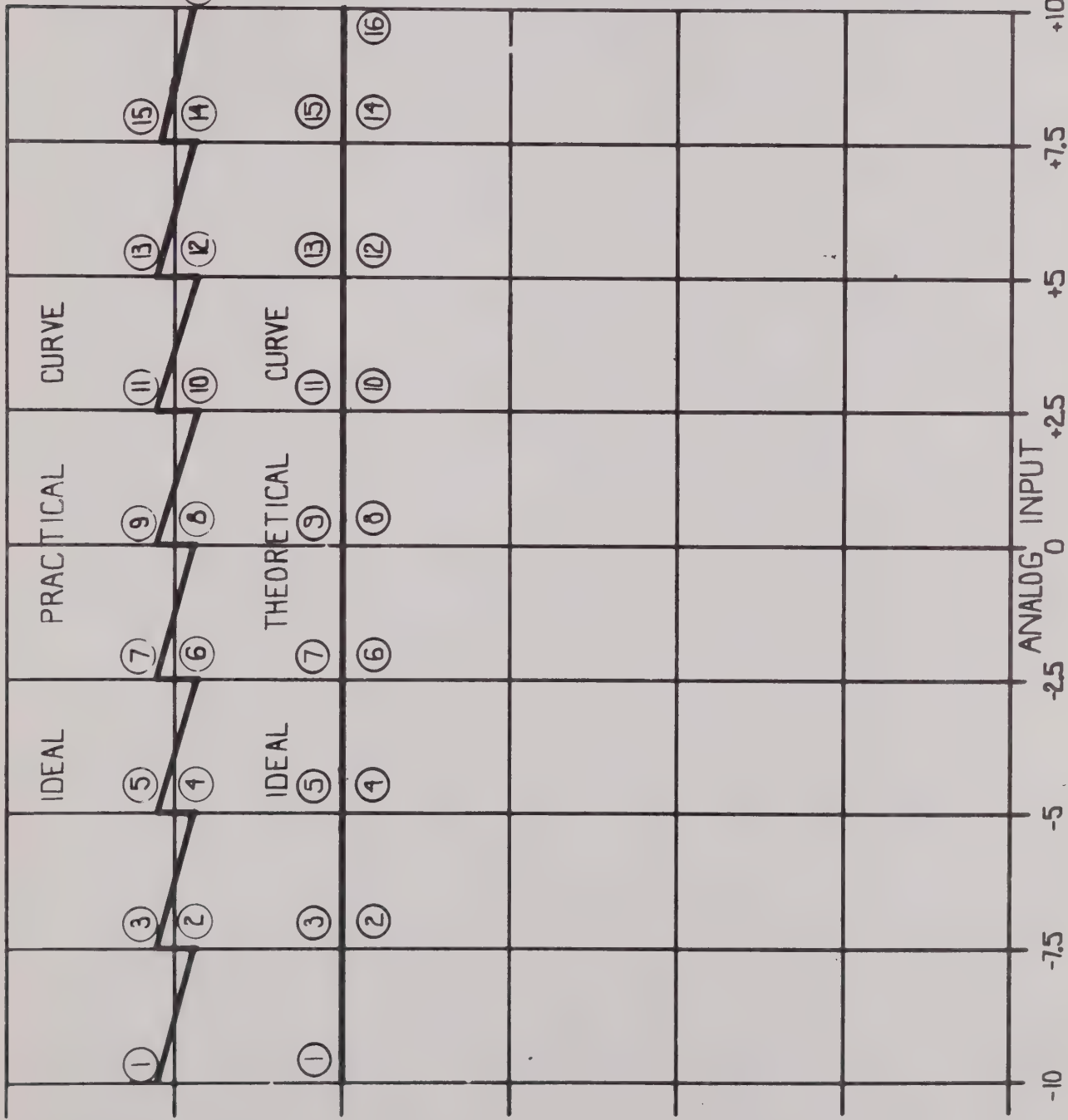
6.9A

6.9B

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV $\pm W$

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ + 2.4920
- ⑪ + 2.5123
- ⑫ + 4.9920
- ⑬ + 5.0123
- ⑭ + 7.4920
- ⑮ + 7.5123
- ⑯ + 9.9920



6.6.3 (continued)

Curves 6.11 to 6.23 B & C show the affect of adjustments on the first three most significant bit boards on the over-all curve.

The 4th "A" board affects the 1/8 sfale increments in a similar manner, the theoretical values are included in the computer printed work sheet (Figure 6.10).

In Table I the codes always display the same pattern for the last 5 bits.

16	ON	
8	OFF	
4	OFF	ON
2	ON	OFF
1	ON	OFF

The mark (——*) on the last 3 bits indicates a binary 3→4 change.

At this point the code is alternating from 3→4 or 1 00
0 11

This can be observed in the ADC int mode directly. Running at normal speed the change can be observed by an equal brilliance of the last 3 indicators. As the input is changed by a small amount the 3 or 4 code will come on. It must not be confused with the binary 7 where all three indicators are solid on. If the exact center is desired a DC voltmeter may be connected across the "4 bit" to gnd. Adjust input so that the 4 bit is on solid. Note voltage. When the meter indicates 1/2 the noted voltage a 50% duty cycle will be present. This means the 4 is on 1/2 the time which in turn means the 2 & 1 are on the other 1/2. This procedure is usually only required where noise makes it difficult to determine the transition point.

6.6.4 /adjustments to Curves

Adjusting the Zero and the B0 potentiometers will remove any transition errors present (see Figure 6.1). These corrections should be made to approach the Ideal Practical Curve in Figure 6.9(a). The actual curve although not as perfectly shaped as the Ideal Curve must be within the tolerance of the ADC. Retain this curve after it is corrected and mark it 25°C. It will be used later as a reference.

Errors at the transition points should always go from minus to positive as input goes from negative to positive: Example points ② & ③ (Figure 6.1). The error at point ③ must be more positive than the error at point ②. If not, corrections are made as required.

Transition width adjustments affect more significant bit transitions. Therefore an adjustment to the 3rd A Board zero will require readjustment of the 1st and 2nd A board zeroes. Zero or B0 adjustments do not affect the slope but slope adjustments do affect zeroes of more significant boards.

After making a change, it is best to re-plot the curve to be sure the desired affect was obtained.

6.6.5 Third "A" Board Adjustments

(a) ZERO: Used to correct transition widths at $\pm 2.5\text{v}$ & $\pm 7.5\text{v}$

If the -7.5080 transition is changed to -7.5084 or minus by .4mv the -7.4877 transition is changed to -7.4873 or positive by .4mv. The width plotted on curve 6.11B is now 1.6mv or .8 greater than curve 6.11A The amount of the increase is twice that of the change made.

6.6.5 (continued)

Curve 6.11A PT2 = -7.5080 or -.4mv error
 PT3 = -7.4877 or +.4mv error
 W = .8mv

Curve 6.11B PT2 = -7.5084 or -.8mv error
 PT3 = -7.4873 or +.8mv error
 W = 1.6mv

If the -7.5080 transition is changed to -7.5076 or positive by .4mv the .4mv the -7.4877 transition goes to -7.4881 or negative by .4mv. The width W is now 0 since both numbers are at the theoretical values. This is shown in curve 1C.

NOTE that changing W at $\pm 3/4$ scale (-7.5v) causes an equal change at $\pm 2.5v$ ($1/4$ scale) and +7.5v ($+3/4$ scale) points. It also affects $\pm 1/2$ scale and zero transition widths. When using zero pot either side of the transition may be used. The other will move the same amount in the other direction.

(b) B0:

The B0 adjustment is only used where positive voltage is at the input of the third A board. It is used at the $\pm 1/4$ & $3/4$ scale points but may only be adjusted one side of the transition instead of either like the zero pot. At $3/4$ scale points (2) or (15) must be used. At $1/4$ scale points (7) or (10) must be used.

If the -7.5080 transition is changed to -7.5085 or .5mv more negative then the -7.4877 transition is unaffected and the transition width W increases from -.8 to -1.3mv error. Example: Curve 6.2 B. If the -7.5080 transition is changed to -7.5072 the width W becomes "0" as in Curve 6.12.

NOTE: When using the B0 adjustment to change W the $\pm 1/2$ scale transition

6.6.5 (continued)

(c) S2:

The S2 adjustment changes slopes per curve 6.13B or 6.13C. The adjustment is made from the end points; (1), (16) or center points 8 or (9).

Example Curve 6.13B:

AT (1) -9.9877 is increased to -9.9867 or 1mv more positive with S2 pot.

NOTE: The 3rd A S2 pot affects the zero transition width. In Curve 6.13B it increases it. The same change would result from adjusting points (8) or (16) 1mv negative or point (9) 1mv more positive.

Curve 6.13B shows the opposite direction change.

NOTE: S2 shows a gain slope change where zero and B0 adjustments show an offset change.

(d) S1:

The S1 adjustment changes slopes per curves 6.14B and 6.14C. Adjustments are made from 1/2 scale transition.

EXAMPLE: Curve 6.14B is obtained from 6.14A by going to pt (4) or (12) and adjusting S1 for about -.6mv more error, or going to point (5) or (13) and adjusting for a positive .6mv error increase. This adjustment changes the width of the $\pm 1/2$ scale transitions.

6.6.6 2nd "A" Board Adjustments

Adjustments are similar to the 3rd "A" board but are made at different points.

The Zero and B0 are used to correct $\pm 1/2$ scale transitions. The affects are shown on Curve 6.15B and 6.15C.

If the -5.0080 transition is changed with the zero pot to -5.0084 (-.4mv) the -4.9877 transition goes to -4.9873 (+.4mv). This widens the transition twice by the amount of change made.

The B0 adjustment like the 3rd board must be made at the side of the transition with a positive voltage into the board. In this case -5.0080 transition or the +5.0123 transition.

The S2 adjustments are made at the $\pm f/s$ transitions.

The S1 adjustments are made at the $\pm$ zero transitions.

6.6.7 1st "A" Board Adjustments

Zero pot offsets both halves of curve in opposite directions per Curve 6.19A. The B0 adjustment offsets the half of the curve with positive voltage into the board.

This means with an inverting buffer between the input and the first "A" board that the negative transition (normally zero -.0080 for example) is used.

The S2 potentiometer pivots the half of the curve with a positive input to the 1st "A" board about zero. The corresponding full scale transition is used for adjustment. Reference Curves 6.21B and C.

The S1 potentiometer pivots the half of the curve with a negative input to the 1st "A" board. The corresponding full scale transition is used for adjustment. Reference Curves 6.22B and C.

6.6.8 High Temperature

- (a) Raise the ambient temperature of the system to 50°C or 55°C as required. Allow the unit to soak at this temperature for a minimum of 1/2 hour.
- (b) Run a 16 point linearity curve plus the transition points around $\pm 7/8$ th scale. (Refer to 6.6.3 16 point linearity).
- (c) Compare these results with the room temperature curve. Using the available drift potentiometers, Zero or B0, make adjustments to return the high temperature results to the results obtained in the 25°C run.

At hi temperature the DRIFT potentiometers on the "A" boards allow corrections to be made corresponding to room temperature Zero and B0. Adjustments are made starting with least significant bit (usually the A4 board at a 1/8 scale transition) toward the msb {A1}. The curve is adjusted to be as close as possible to the one at room temperature.

In addition to the "A" boards, the buffer/or sample-and-hold have zero drift potentiometers and the $\pm$ reference power supply have drift potentiometers to correct their outputs.

The buffer (sample-and-hold) drift potentiometers shift the entire curve in the same manner as Curve 6.23B. Since it may not be possible to separate ADC drift from buffer drift, it is sometimes more expedient to attach a wire to the buffer output to a voltmeter. At room temperature, the buffer can be set for a " 0 volts in - 0 volts " out state. At high temperature buffer zero drift potentiometer can

6.6.8(c) (continued)

be used to repeat this condition. Remaining offset is then due to ADC which can be removed via the B0 and Zero Drift potentiometers 1st "A" boards.

In Figure 6.24B the curve has been corrected to this point which includes an undesirable zero offset and could not be corrected to proper zero with the buffer drift potentiometer. However, this may not be the cause of drift. If the buffer is reset (as indicated above) to Zero Volts out with Zero Volts in by the drift potentiometer the true cause can be seen.

CASE I: If the curve then returns to room temperature position the buffer drift caused offset.

CASE II: If not, the curve will still be offset in the same or some other position. The cause may be a combination of first A Zero and B0 shift and can be corrected with these drift potentiometers.

Suppose with the buffer drift set to Zero, the curve is approximately as shown (Curve 6.24B). Zero transition points (8), (9) would be approxi-

mately	(8)	-.0066	or +1mv error
	(9)	+.0137	or +1.4mv error

The 1st "A" board Zero and B0 drift potentiometers can be used to offset the curve back around zero as follows:

First determine whether buffer or S/H is inverting. The B0 adjustment is only made with positive voltage into the 1st "A" board and only affects the corresponding half of the curve. The zero adjustment affects both halves equally and may be made with either polarity input. Reference curves 6.19B and C, 6.20B and C.

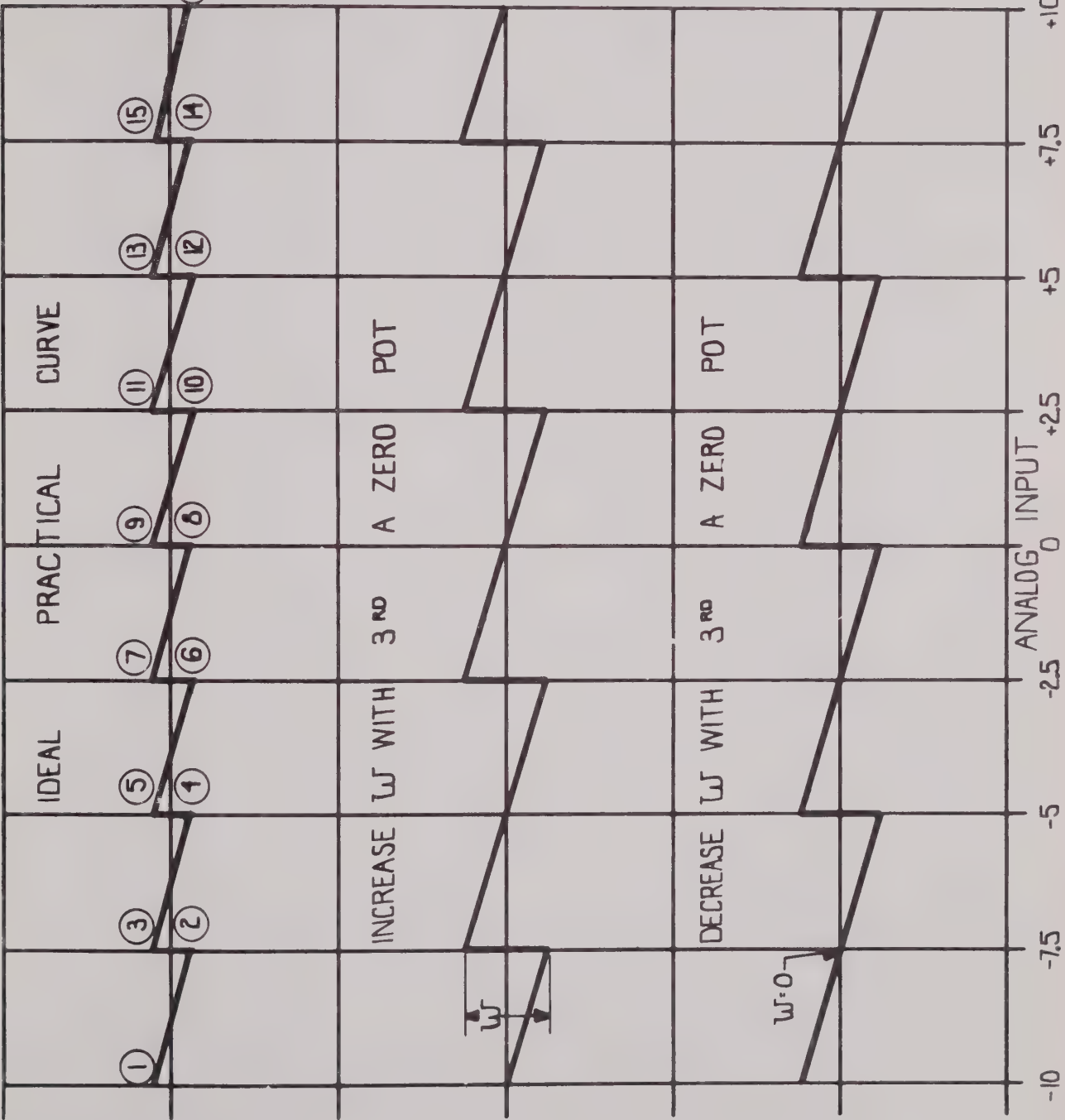
6.6.10 (continued)

- (e) Return ADC to hi temperature to dry out if moisture was present.
Allow 1/2 hour minimum time to settle.
- (f) Return ADC to room temperature and allow a 1 hour minimum time to settle. Repeat 16 point curve. If specific bit is to be widened make required adjustments to do this and others as required to correct curve.

ERROR
(MV)

+2
+1
0
-1
-2

6.11A



6.11B

6.11C

ANALOG INPUT

-10 -7.5 -5 -2.5 0 +2.5 +5 +7.5 +10

ERROR
(MV)

+2
+1
0
-1
-2

6.12 A

INCREASE ω WITH

3RD

A B.O.

POT

6.12 B

ω

DECREASE ω WITH

3RD

A B.O.

POT

6.12 C

$\omega = 0$

IDEAL

PRACTICAL

CURVE

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV- ω

- ① -9.9877
- ② -7.5080
- ③ -7.4177
- ④ -5.0080
- ⑤ -4.9377
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ +2.4920
- ⑪ +2.5123
- ⑫ +4.9920
- ⑬ +5.0123
- ⑭ +7.4920
- ⑮ +7.5123
- ⑯ +9.9920

ANALOG INPUT

-10

-7.5

-5

-2.5

0

+2.5

+5

+7.5

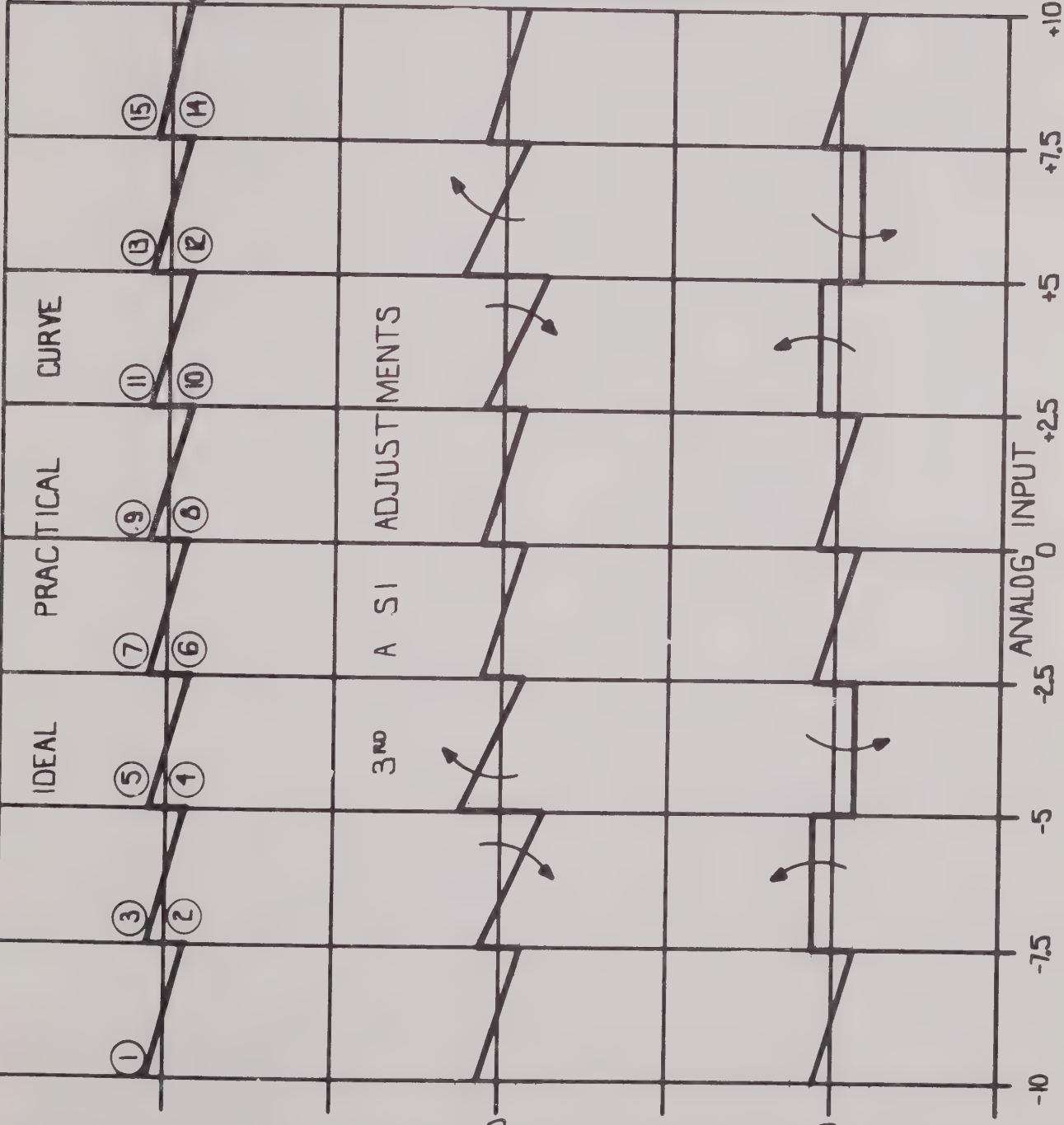
+10

ERROR
(MV)
+2
+1
0
-1
-2

6.14 A

6.14 B

6.14 C



EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV-V_S

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ +2.4920
- ⑪ +2.5123
- ⑫ +4.9920
- ⑬ +5.0123
- ⑭ +7.4920
- ⑮ +7.5123
- ⑯ +9.9920

ERROR
(mV)

6.15A

6.15B

6.59

	IDEAL	PRACTICAL	CURVE
1. Definition	A theoretical model of a system or process, often based on idealized assumptions.	A model that takes into account real-world constraints and limitations.	A graph or diagram showing the relationship between variables, often used to compare ideal and practical performance.
2. Assumptions	Often based on idealized assumptions, such as perfect materials, perfect information, or perfect control.	Often based on realistic assumptions, such as imperfect materials, imperfect information, or imperfect control.	Often used to show the deviation from ideal performance due to practical constraints.
3. Applications	Used in theoretical analysis and design to establish a baseline or target performance.	Used in practical design and analysis to predict system behavior under real-world conditions.	Used to visualize the performance gap between ideal and practical results.
4. Limitations	May not accurately represent real-world behavior due to idealized assumptions.	May be more complex and difficult to analyze than ideal models.	Often used to highlight the limitations of ideal models.

CURVE

PRACTICAL

IDEAL

INCREASE WITH

22

A ZERO

POT

DECREASE

WITH HIM

22

A ZERO

POT

 $\sqrt{0.71}$

ANALOG INPUT

25

+

+75

 $\frac{1}{10}T$

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV-2W

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ + 2.4920
- ⑪ + 2.5123
- ⑫ + 4.9920
- ⑬ + 5.0123
- ⑭ + 7.4920
- ⑮ + 7.5123
- ⑯ + 9.9920

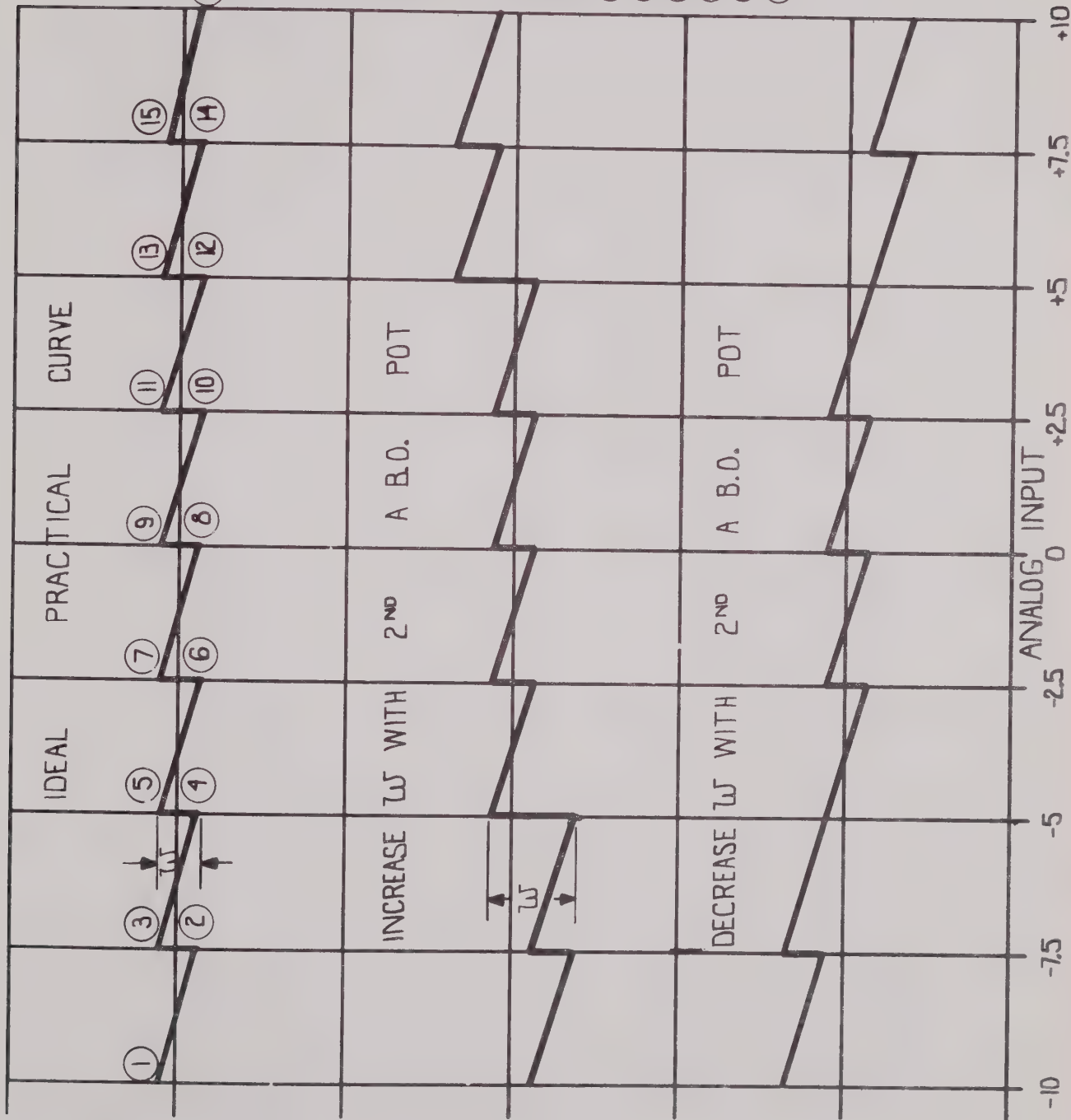
ERROR
(MV)

+2
+1
0
-1
-2

6.16A

6.16B

6.16C



EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV ω

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ +2.4920
- ⑪ +2.5123
- ⑫ +4.9920
- ⑬ +5.0123
- ⑭ +7.4920
- ⑮ +7.5123
- ⑯ +9.9920

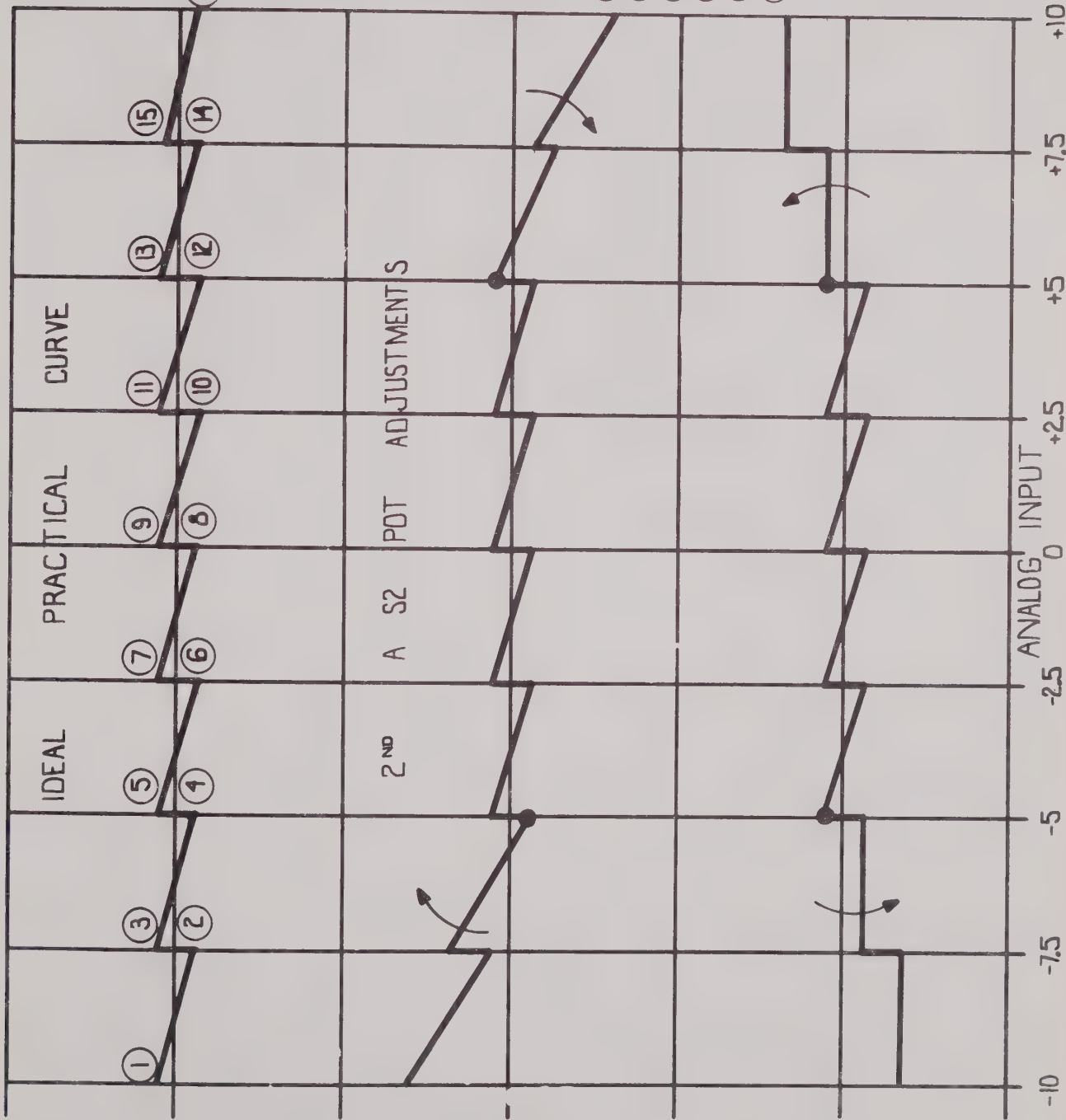
ERROR
(MV)

+2
+1
0
-1
-2

6.17A

6.17B

6.17C



ANALOG INPUT

-10

-7.5

-5

-2.5

0

+2.5

+5

+7.5

+10

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV $\cdot W$

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ + 2.4920
- ⑪ + 2.5123
- ⑫ + 4.9920
- ⑬ + 5.0123
- ⑭ + 7.4920
- ⑮ + 7.5123
- ⑯ + 9.9920

ERROR
(MV)

+2
+1
0
-1
-2

6.18 A

6.18 B

6.18 C

CURVE

PRAC TICAL

IDEAL

ANALOG INPUT

-10

-7.5

-5

-2.5

0

+2.5

+5

+7.5

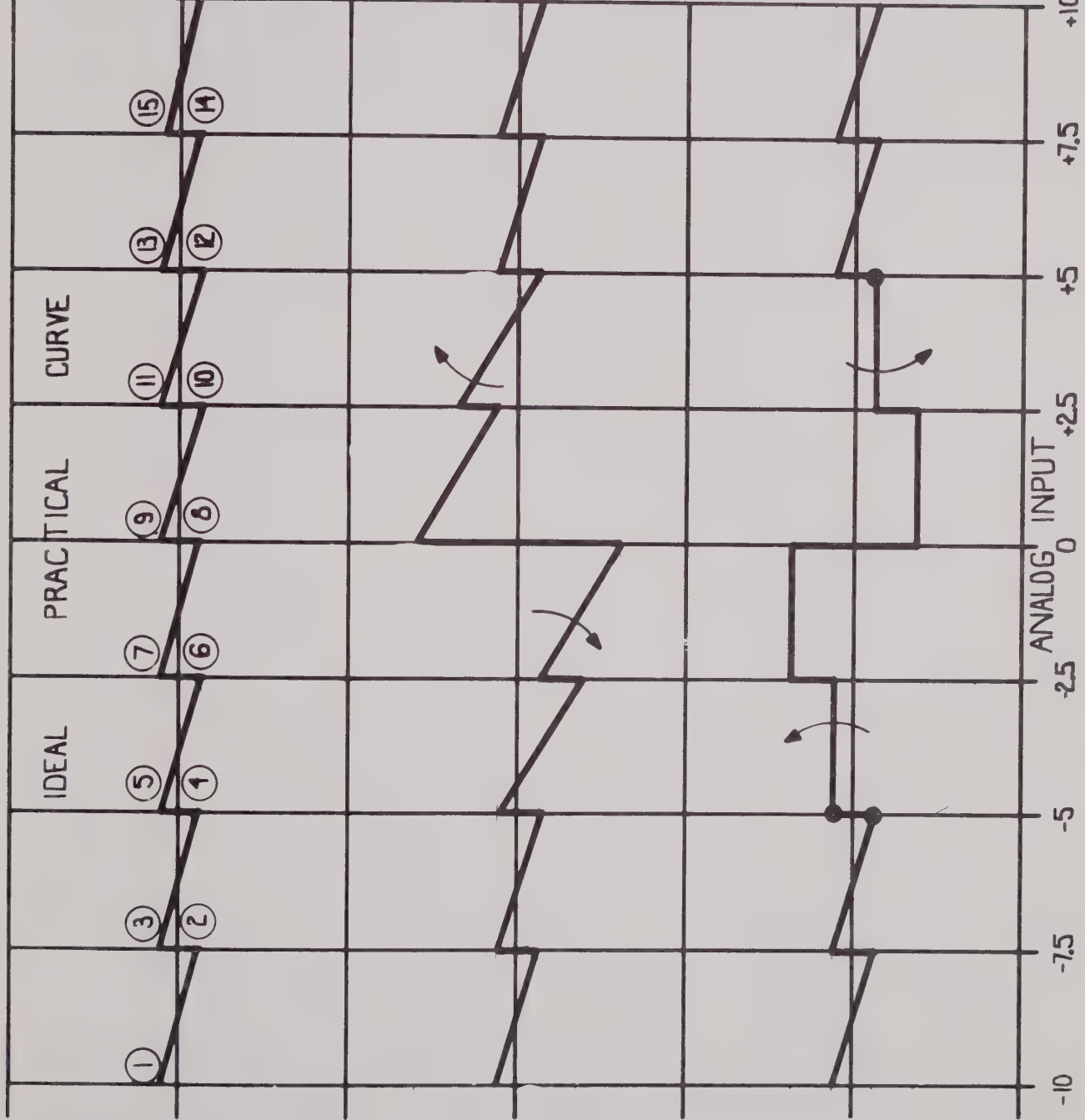
+10

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV-VW

16

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ +2.4920
- ⑪ +2.5123
- ⑫ +4.9920
- ⑬ +5.0123
- ⑭ +7.4920
- ⑮ +7.5123
- ⑯ +9.9920



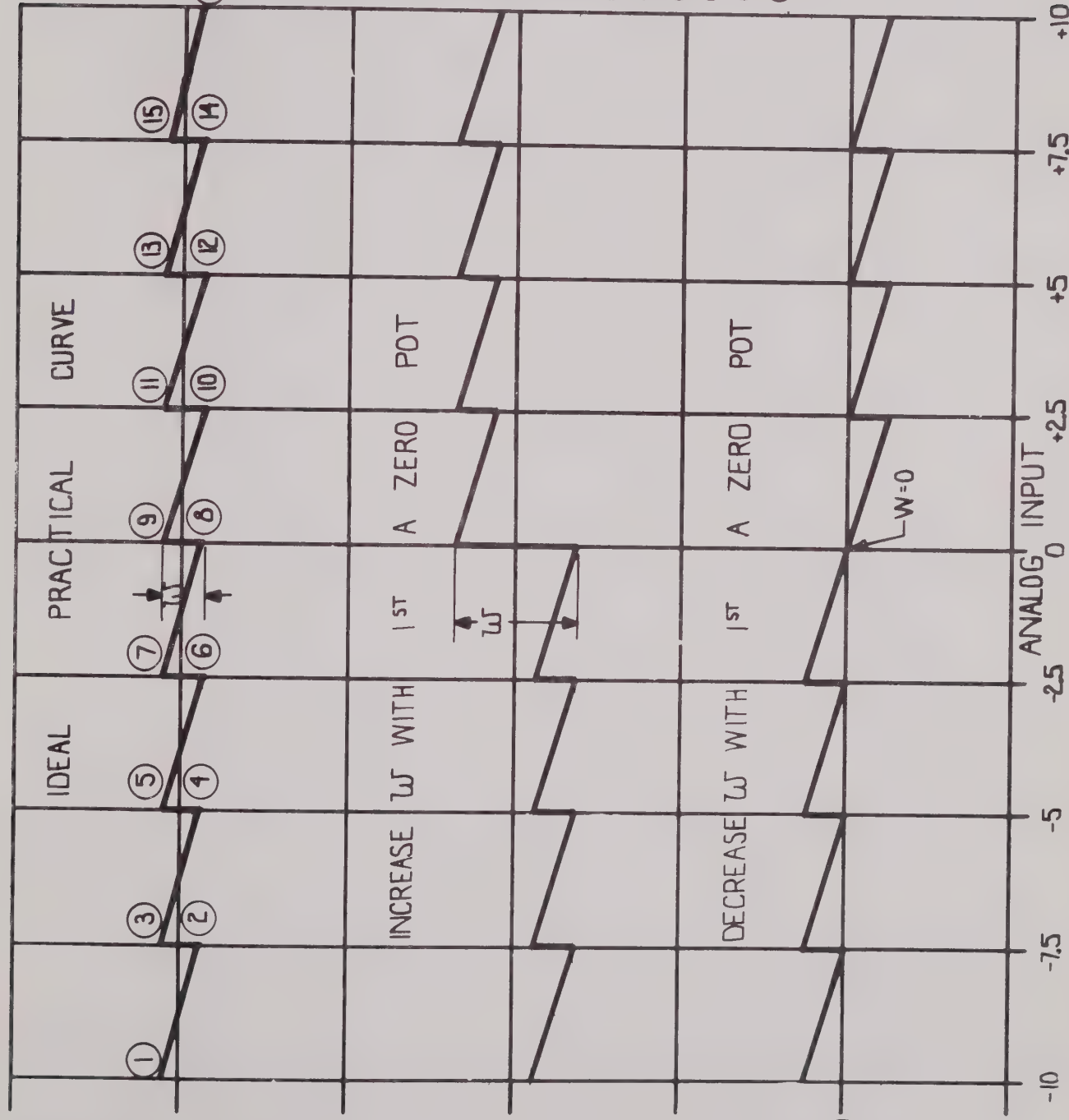
ERROR
(MV)

+2
+1
0
-1
-2

6.19 A

6.19 B

6.19 C



ANALOG INPUT

-10 -7.5 -5 -2.5 0 +2.5 +5 +7.5 +10

EXAMPLE
FOR $\pm 10V$ F/S

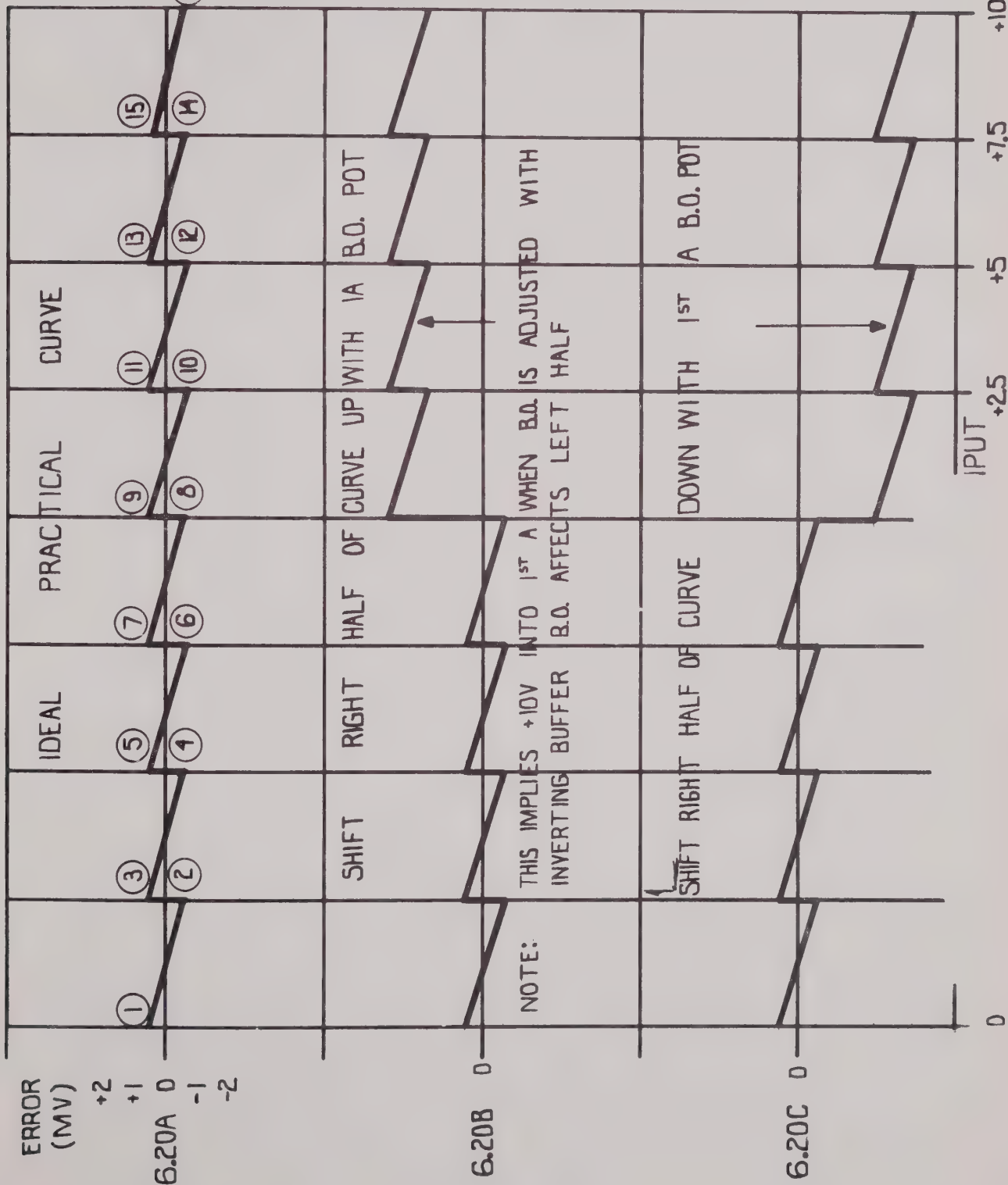
TYP VALUES
.8MV-W

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ +2.4920
- ⑪ +2.5123
- ⑫ +4.9920
- ⑬ +5.0123
- ⑭ +7.4920
- ⑮ +7.5123
- ⑯ +9.9920

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV/V

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ +2.4920
- ⑪ +2.5123
- ⑫ +4.9920
- ⑬ +5.0123
- ⑭ +7.4920
- ⑮ +7.5123
- ⑯ +9.9920



ERROR
(MV)

+2
+1
0
-1
-2

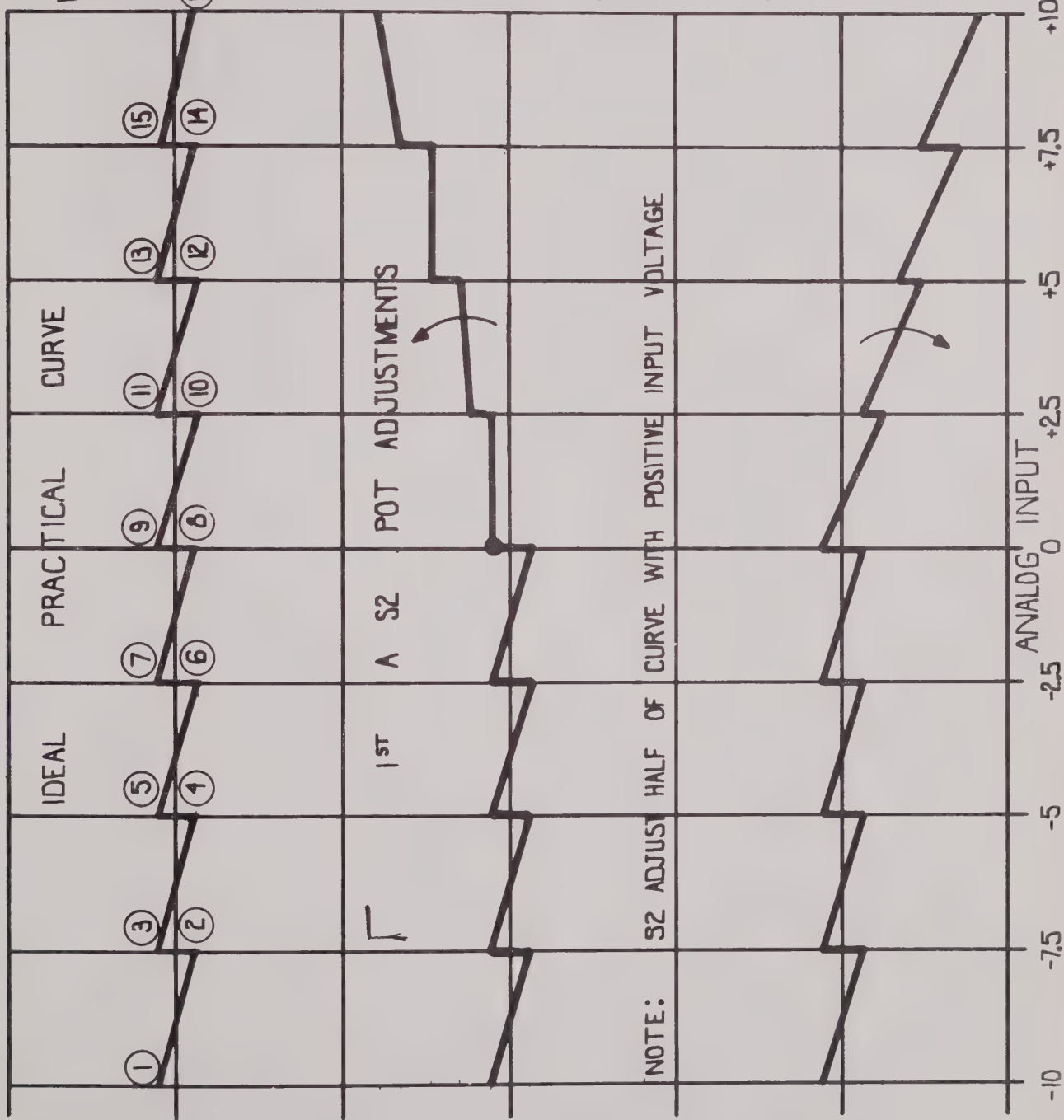
6.21A

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV/V

(16)

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ + 2.4920
- ⑪ + 2.5123
- ⑫ + 4.9920
- ⑬ + 5.0123
- ⑭ + 7.4920
- ⑮ + 7.5123
- ⑯ + 9.9920



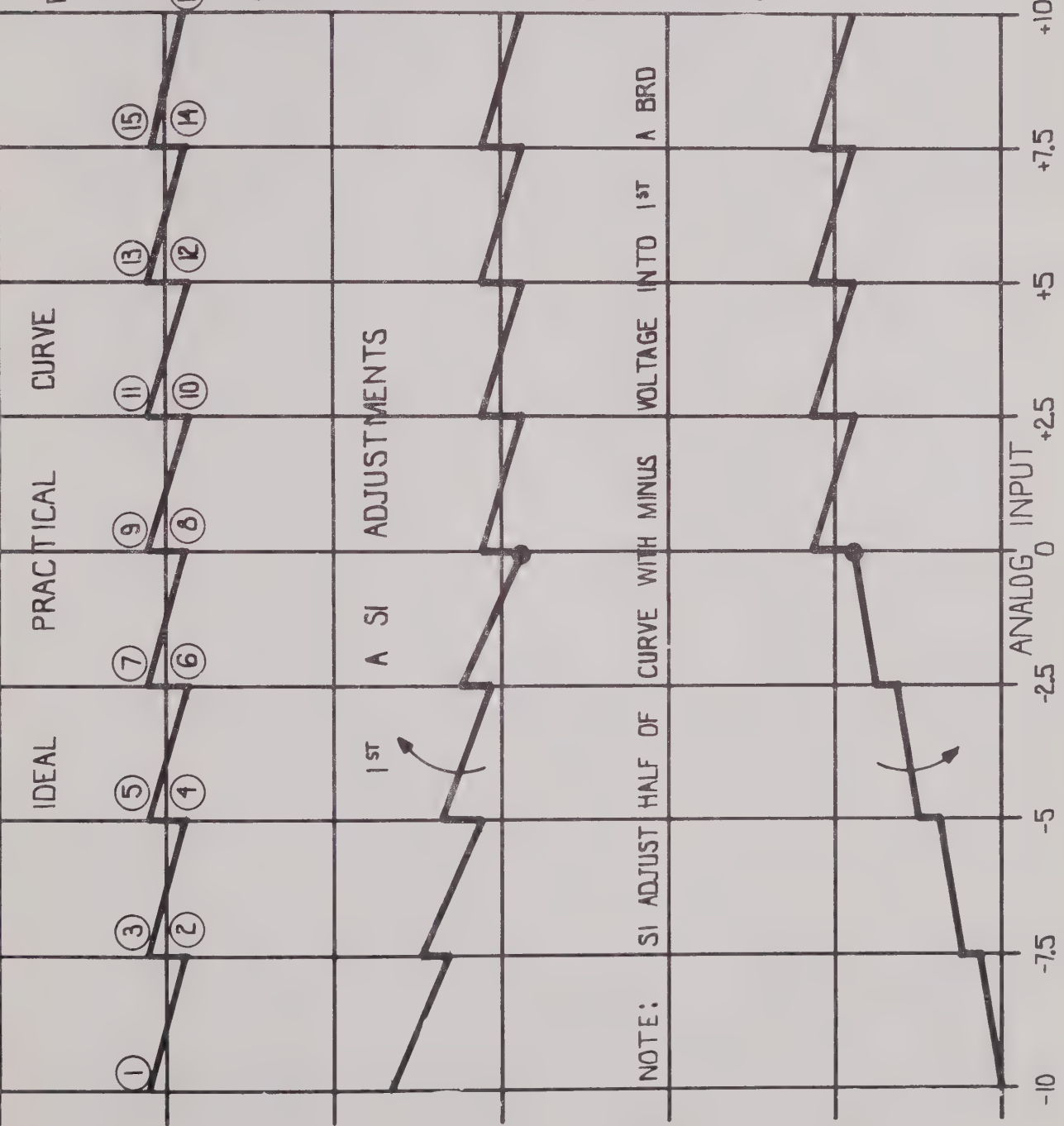
-10 -7.5 -5 -2.5 0 +2.5 +5 +7.5 +10

ERROR
(MV)
+2
+1
0
-1
-2

6.22A

6.22B

6.22C



EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV-U

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ +2.4920
- ⑪ +2.5123
- ⑫ +4.9920
- ⑬ +5.0123
- ⑭ +7.4920
- ⑮ +7.5123
- ⑯ +9.9920

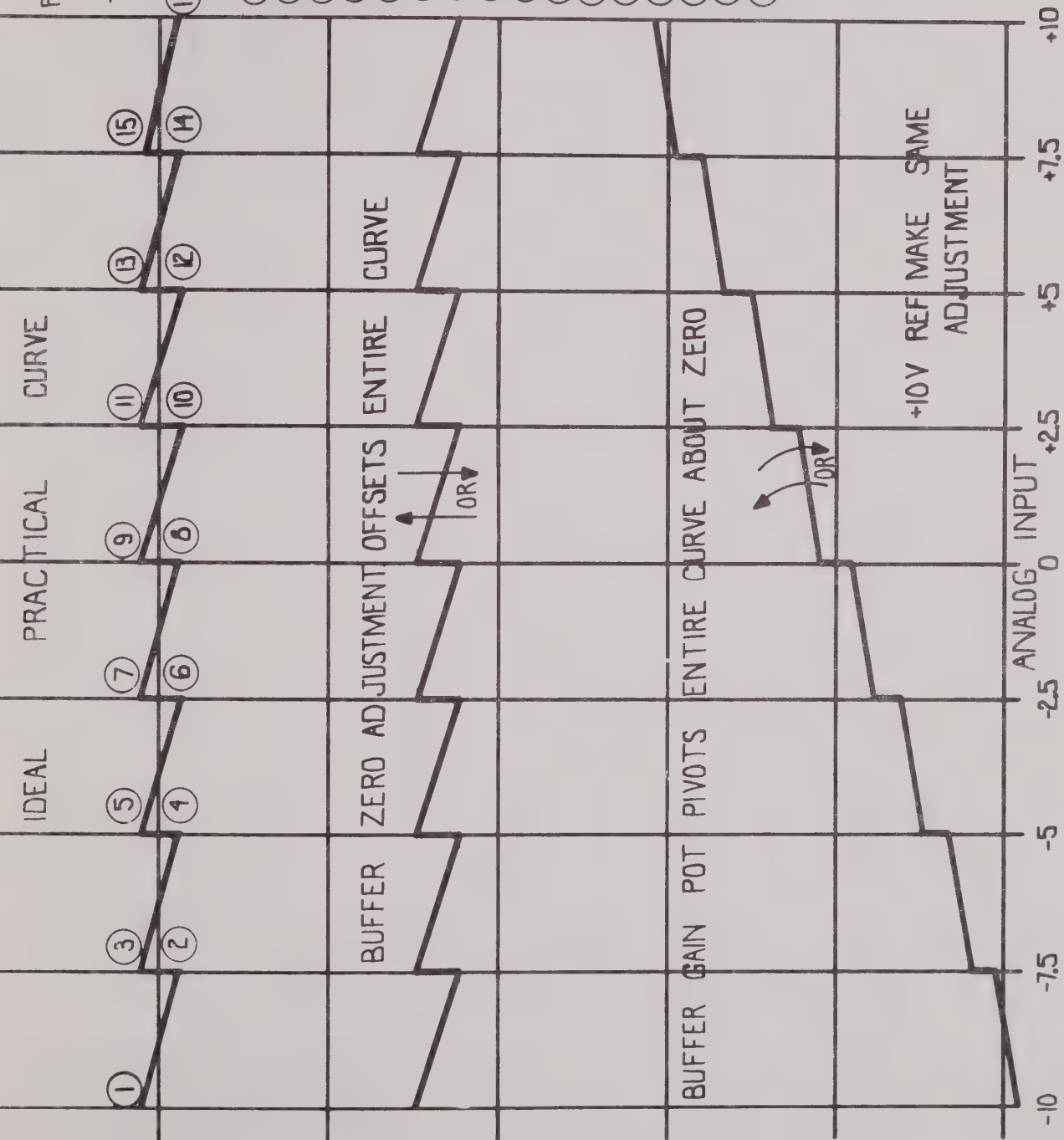
ERROR
(MV)

+2
+1
0
-1
-2

6.23A

6.23B

6.23C

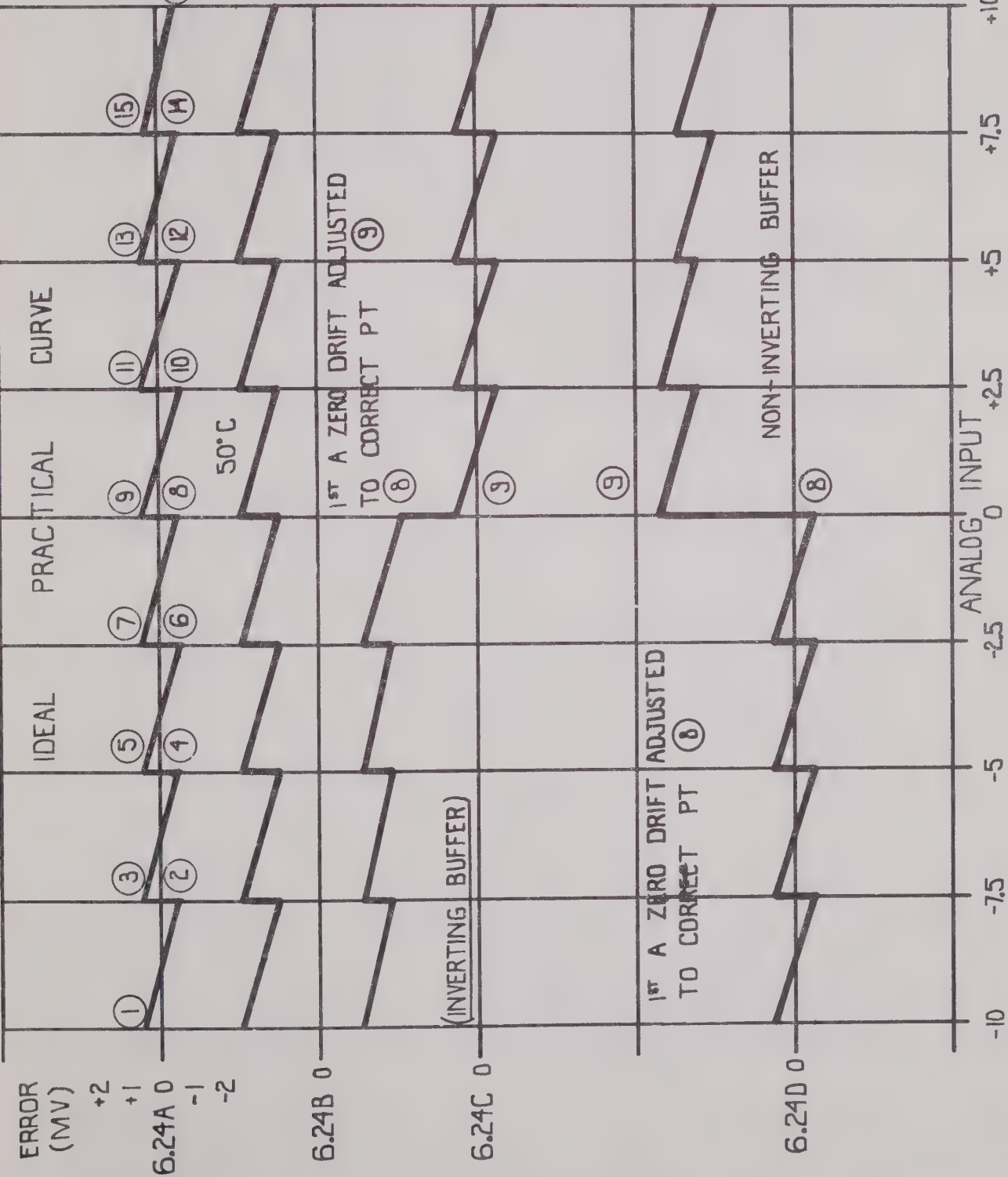


EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV- ω

- 1 -9.9877
- 2 -7.5080
- 3 -7.4877
- 4 -5.0080
- 5 -4.9877
- 6 -2.5080
- 7 -2.4877
- 8 - .0080
- 9 + .0123
- 10 +2.4920
- 11 +2.5123
- 12 +4.9920
- 13 +5.0123
- 14 +7.4920
- 15 +7.5123
- 16 +9.9920

EXAMPLE
FOR $\pm 10V$ F/S
TYP VALUES
.8MV- μ

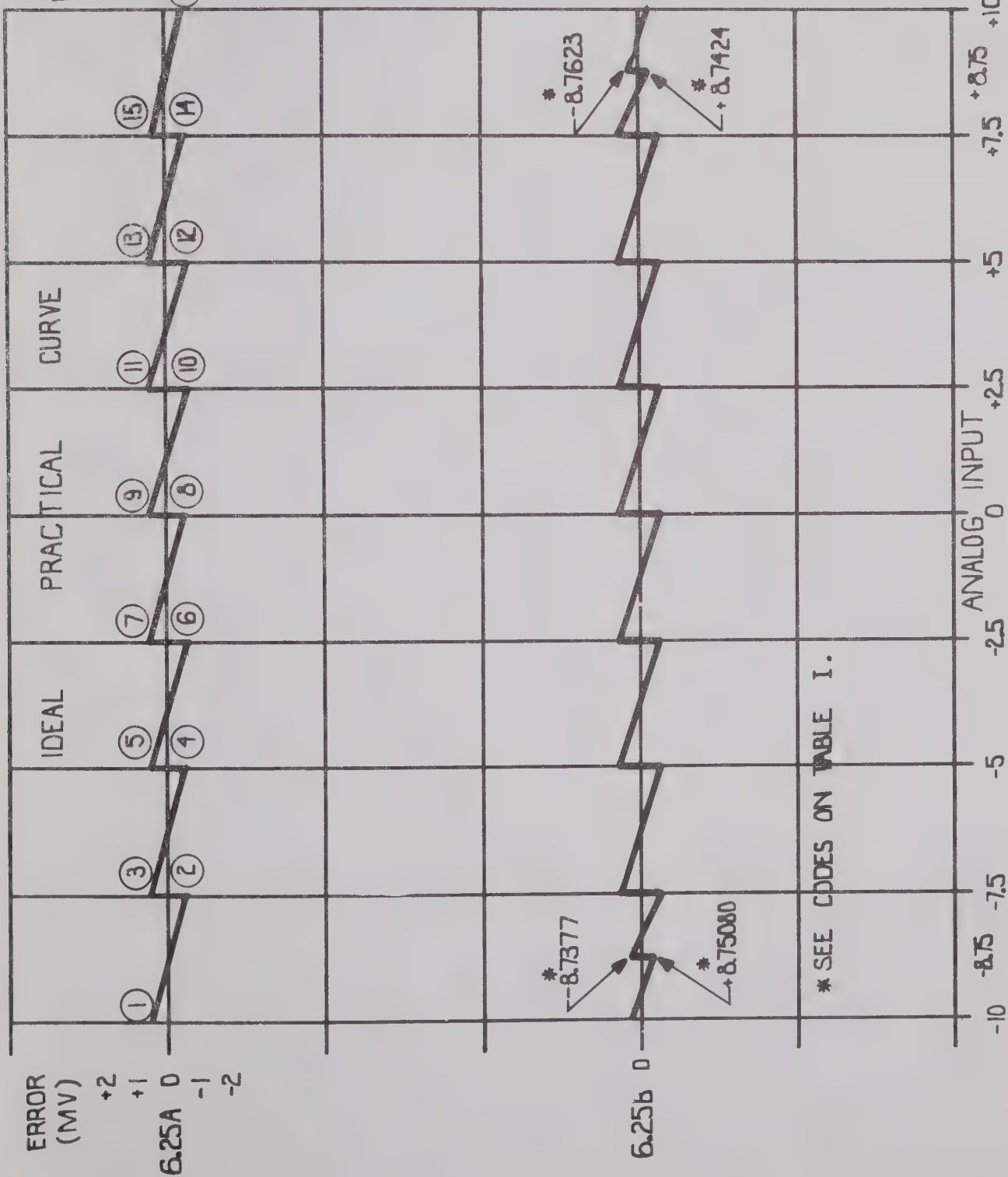


- 1 -9.9877
- 2 -7.5080
- 3 -7.4877
- 4 -5.0080
- 5 -4.9877
- 6 -2.5080
- 7 -2.4877
- 8 - .0080
- 9 + .0123
- 10 +2.4920
- 11 +2.5123
- 12 +4.9920
- 13 +5.0123
- 14 +7.4920
- 15 +7.5123
- 16 +9.9920

EXAMPLE
FOR $\pm 10V$ F/S

TYP VALUES
.8MV- ω

- ① -9.9877
- ② -7.5080
- ③ -7.4877
- ④ -5.0080
- ⑤ -4.9877
- ⑥ -2.5080
- ⑦ -2.4877
- ⑧ - .0080
- ⑨ + .0123
- ⑩ + 2.4920
- ⑪ + 2.5123
- ⑫ + 4.9920
- ⑬ + 5.0123
- ⑭ + 7.4920
- ⑮ + 7.5123
- ⑯ + 9.9920



SECTION 7

TROUBLE SHOOTING PROCEDURES

7.1 SYSTEM TROUBLE SHOOTING

This section describes the recommended procedures for trouble shooting the GM Series Multiplexing Analog-to-Digital Conversion System. The procedures have been separated into three major building blocks of the system i.e. (1) the power supply; (2) the multiplexer; (3) the analog-to-digital converter.

Prior to beginning the trouble shooting, make certain that all instrumentation associated with the system is checked to determine that the apparent problem is within the GM System. Check that all external addressing is correct and that the input/output, analog and digital lines are properly terminated.

Calibration adjustment potentiometers and capacitors are preset at the factory. No adjustment of these controls should be attempted until a check of the system has been made.

To prevent damage to the semiconductors the main power should be turned off before plugging or unplugging any circuit card.

In some cases, concerning the Sample-and-Hold Buffer Amplifier, timing board, or high resolution bit boards placing the board on an extender card will effect the normal operation of that board. All boards should be in their slots when any critical parameters are measured such as system timing, sample-and-hold adjustments and final calibration.

7.1 (continued)

This system has a temperature sensitive switch mounted internally at the rear of the chassis. This switch is designed to interrupt the main power should the internal temperature of the system rise to 70°C. This temperature switch is self-resetting and will restore the power when the temperature is again lowered to 55°C.

7.2 GENERAL TROUBLE SHOOTING EQUIPMENT

Equipment recommended for trouble shooting consists of the following:

- (a) A stable DC analog voltage source, variable over the range of $\pm$ full scale input voltage or ± 10 volts whichever is greater. The voltage resolution should be at least 25% of the least significant bit. The source impedance should be less than 1000 ohms.
- (b) Oscilloscope, Tektronix 545A, with 1A5 and CA Preamplifiers, or equivalent.
- (c) Five-digit digital voltmeter, differential voltmeter, or equivalent. The accuracy should be at least twice that of the system being tested.
- (d) Triangle wave generator with a capability of 20 volts peak-to-peak into a 470 ohms load at 1 kHz.
- (e) Volt ohmmeter such as Simpson 260.
- (f) Pulse generator to provide clock pulses of an equivalent in amplitude width and frequency to the normal system operating pulses.
- (g) Printed circuit card extender, bit board extender (Part No. 52315) and Sample-and-Hold Buffer extender (Part No. 52318). All three are supplied with the unit. (Part No. 52315 and 52318 may be replaced by a single extender Part No. 52330.)

7.3 POWER SUPPLY

	<u>INDICATION</u>	<u>CHECK</u>
7.3.1	Loss of Power	Line fuse, power, ON-OFF Switch, High temperature which may have caused temperature sensor to remove power.
7.3.2	Loss of Data Output Bit display on Front Panel	Assuming that the ADC is operating correctly, and the failure is other than an individual LED, the lamps are connected through resistors to the common 5 volt supply. Check the 5 volt supply.
7.3.3	Loss of Individual Display Bit on Front Panel	The display is accomplished by using an LED device, they are driven by the output data through inverters mounted on the lamp display board. To turn the lamp on the inverter output must go false. Check both input drive to the inverter and the output of the inverter. If the above checks prove "OK" then the lamp is at fault.
7.3.4	Non-Operating System	First check to see that all plug-in boards are seated properly. If the above check has been made and the problem still exists make a check of the plus and minus 10 volts and the plus and minus 33 volts. Refer to Figure 7.4 for these test point locations.

7.4 ADC PROBLEMS AND POSSIBLE SOLUTION

Refer to the Block Diagram, Figure 7.2 for a flow-chart relating to ADC problems and their solutions, by category.

7.4.1 Faulty Positive Reference Power Supply

The reference power supply provides a precisely regulated, highly stabilized reference voltage for use in the ADC bit boards. It consists of two differential amplifiers; each is an operational amplifier with its own feedback loop. The primary standard reference is a zener diode. The reference control -10v adjusts the output voltage of the minus supply, and the +10v control adjusts the output voltage of the plus supply.

A faulty positive reference supply will have the following indications:

- (a) An error in the digital information (gain error).
- (b) A zero offset which cannot be removed with front panel adjustment.

Check the +10 volt reference supply at the test points on the circuit board. It should be adjustable with the gain potentiometer located on that board and labeled +10v.

7.4.2 Faulty Negative Reference Supply

A faulty negative reference supply will give a Zero error, except that the Gain will not be affected. Make the same checks as in Section 7.4.1, using the negative test point (-10v) and adjustment potentiometer. (REF).

7.4.3 Incorrect Calibration of Buffer or Sample-and-Hold Amplifiers

Incorrect data and zero offsets may be due to adjustments in the analog area of the ADC such as the buffer or the Sample-and-Hold Amplifiers.

Check the calibration of the buffer or Sample-and-Hold Amplifiers to see if the problem exists in this area. If the buffer or Sample-and-Hold Amplifiers are not at fault and the reference power supplies have been ruled out as the problem area, refer to Section 7.4.4.

7.4.4 Defective Bit Board

An incorrect digital output may be caused by an uncalibrated bit board or by some malfunction of a bit board.

Check the bit board in question by using the calibration procedure described in Section 3 (only that portion describing the method for introducing a signal into the bit board in question on the plain extender, Part No. 48289, so that test points of individual parts on the board may be available.

Introduce a 1000 Hz triangular wave of a peak-to-peak value of 20v (see Figure 7.3) into the bit board and view the output of the board at A1 and A2.

Trigger the ADC for a conversion at a rate of 10 kHz. The result is shown for a good board in Figure 7.3. Also refer to Figures 4.2 and 4.3 for clarification.

7.5 TROUBLE SHOOTING THE MULTIPLEXER CARD

Refer to Section 2 of this manual for the operation of the multiplexer switch and its associated circuitry. Decide whether the problem which exists is isolated to a particular channel or is common to all multiplexer channels.

Each multiplexer card has its own power regulator and is independent of the other multiplexer cards in this respect. If a particular channel is not functioning, or if only one channel is operating correctly, manually select that channel and monitor the multiplexer drive (see Figure 2.3); check to see that the proper drive signal appears at this test point.

If a drive signal appears at this point, trace the drive and check to see that the correct drive appears at the gate of the FET. The gate is held at a negative potential when the FET is in the OFF state and when it is turned ON, the FET gate is allowed to slew to the same potential as the input signal of the multiplexer.

If the negative potential that holds the gate in the OFF state is functioning properly and the gate does not assume the potential in the input signal, the problem is probably associated with the unity gain amplifier (see Figure 2.3).

If all of the above items checked are functioning correctly, the problem is probably a defective FET semiconductor.

7.6 SPECIFIC MULTIPLEXER PROBLEMS

Below are some problems that may occur; the problem may affect the entire unit and symptoms may appear on all channels, but are caused by a single channel.

7.6.1 Shorted FET Semiconductor Switch

A FET switch that is shorted or fails to turn off completely will provide added analog information to the multiplexer output. If the unit is an ADC/MUX combination, the information out of the ADC will be erroneous and it may appear that the ADC is at fault. When a shorted FET switch is encountered, it may not be immediately apparent. The front panel indication may function correctly and the logic associated with the shorted FET switch may operate correctly, but the analog information on the multiplexer will be incorrect due to the addition of the information of the defective channel.

7.6.2 Open FET Semiconductor Switch

The front panel indication of a selected channel will not always mean that a particular channel is operating properly.

To check the operation of a single channel, move the MODE Switch to the SEQUENTIAL TEST MANUAL position. Set the MUX ADDRESS to cover all channels. Buss all inputs to the same known analog input and monitor the multiplexer output. Manually sequence through each channel, noting that the proper analog signal appears on the multiplexer output for each channel selected. When the correct signal fails to appear on the multiplexer output, the defective channel has been located. Make sure that the test for correct drive for that channel has also been made.

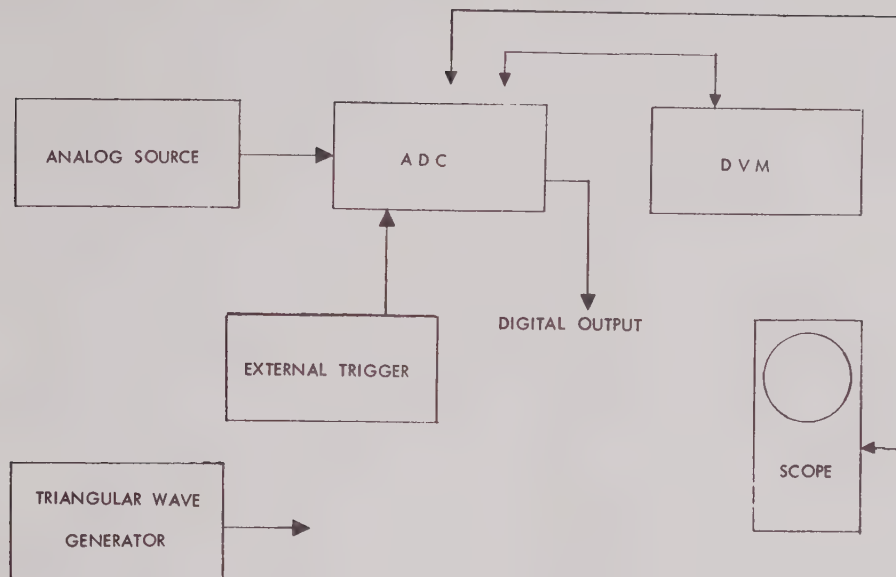


FIGURE 7.1
BENCH TEST SETUP

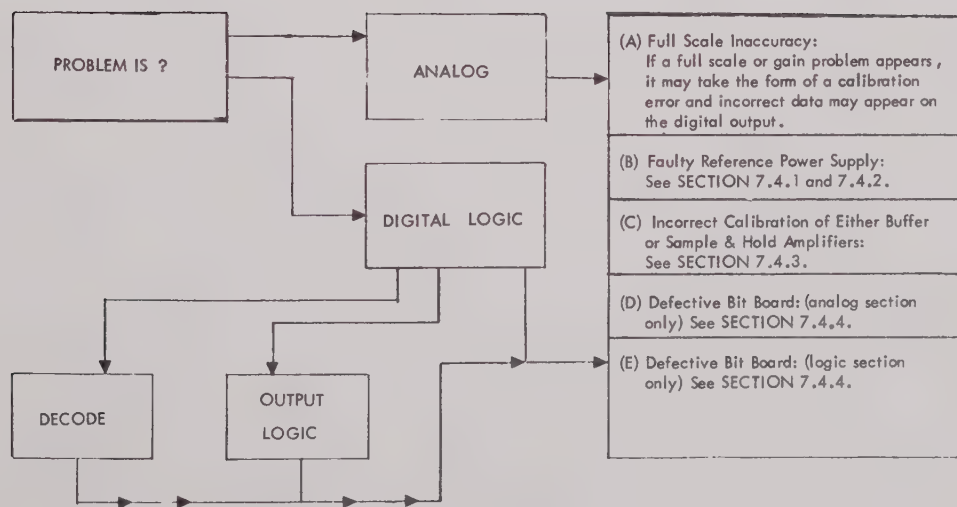


FIGURE 7.2
TROUBLESHOOTING FLOW BLOCK DIAGRAM

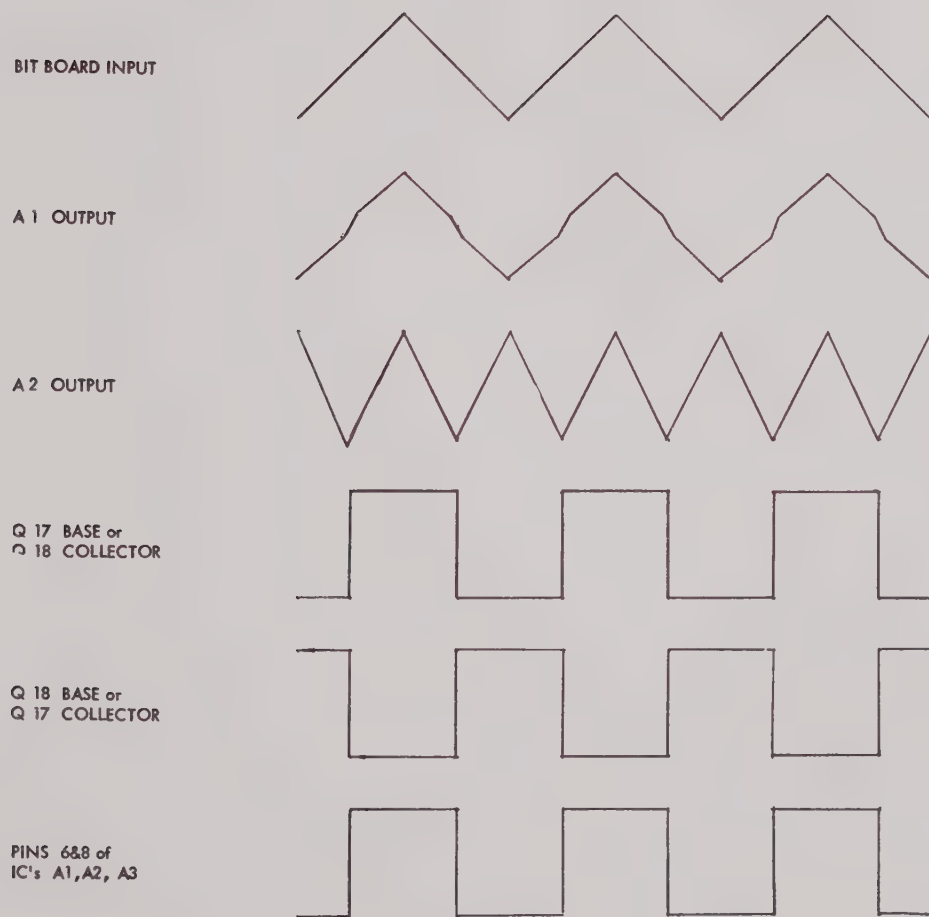


FIGURE 7.3
BIT BOARD TYPICAL WAVEFORMS

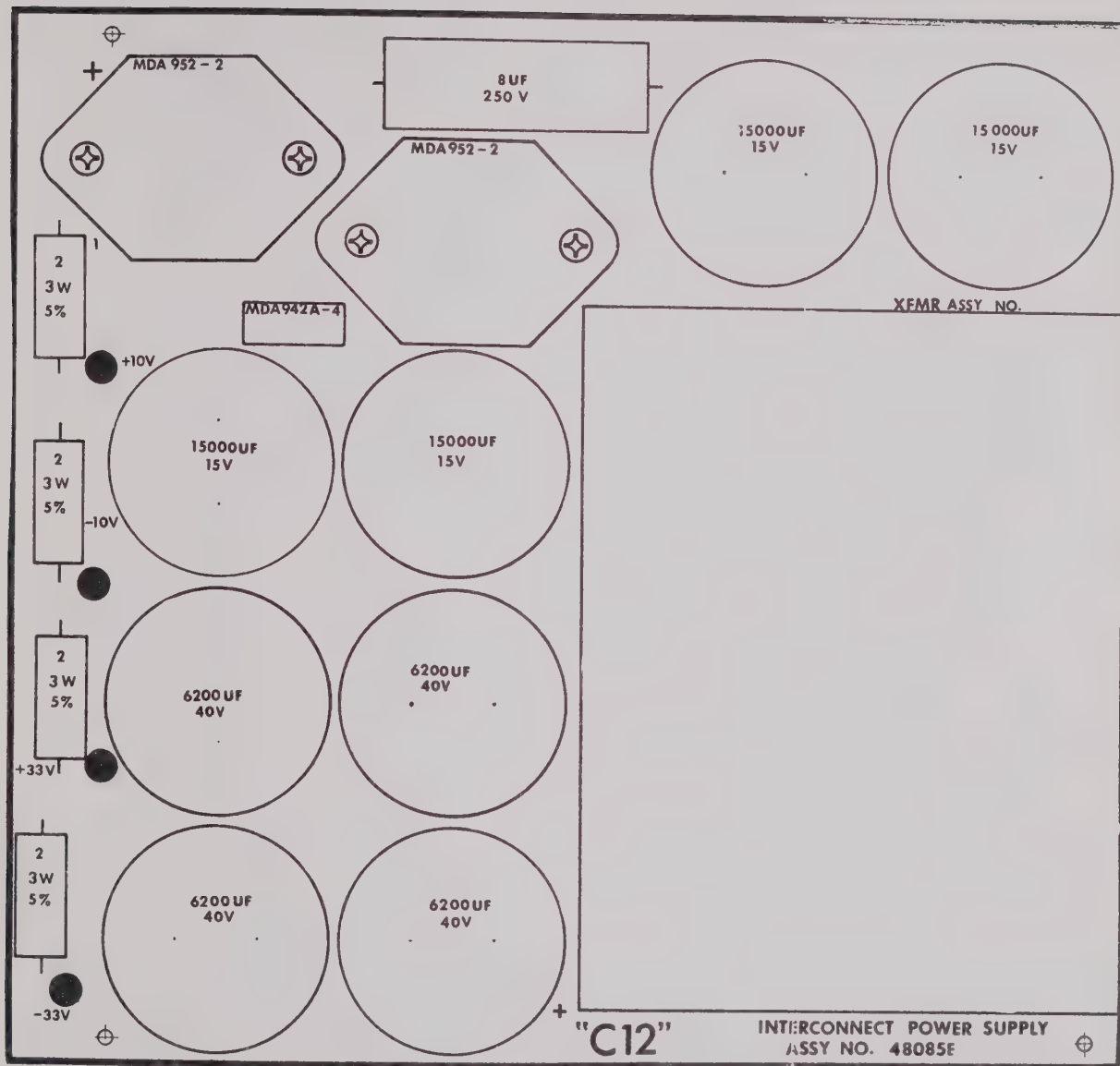


FIGURE 7.4

POWER SUPPLY TEST POINTS

PART NO.	QTY	PRICE	DESCRIPTION			
8-02	5	.79	JACK TIP RED			
8-03	1	.56	JACK TIP BLACK			
8-05	1	3.73	CHOKE	1/4W 10%	2.20H	
8-07	1	.52	CHOKE	1/2W 10%	5.60H	
43-05	24	.01	PUSHNUT			
43-06	2	.02	PUSHNUT			
47-01	2	.52	CAPACITOR		1PF	
47-02	18	.48	CAPACITOR		2PF	
48-00	19	.44	CAPACITOR		3PF	
50-00	1	.48	CAPACITOR		5PF	
50-01	58	.15	CAPACITOR		5PF	
52-01	62	.13	CAPACITOR	5%	10PF	
53-02	2	.23	CAPACITOR	5%	15PF	
55-01	4	.15	CAPACITOR	5%	22PF	
56-01	4	.44	CAPACITOR	5%	30PF	
58-01	5	.34	CAPACITOR	10%	47PF	
60-01	1	.33	CAPACITOR	10%	68PF	
61-01	29	.23	CAPACITOR	10%	100PF	
63-02	1	.34	CAPACITOR	10%	150PF	
64-01	1	.40	CAPACITOR	5%	200PF	
67-01	3	.24	CAPACITOR	10%	220PF	
68-03	1	.48	CAPACITOR	10%	330PF	
72-01	29	.23	CAPACITOR	10%	470PF	
76-00	1	1.18	CAPACITOR	5%	1000PF	
76-02	1	.46	CAPACITOR	20%	1000PF	
77-01	2	3.10	CAPACITOR TRIMMER		9-35PF	

MANUFACTURER MANUFACTURER'S PART NO.

JOHNSON E F	105-602
JOHNSON E F	105-603
MILLER J W	9240-712
MILLER J W	9330-18
PALNUT	PR312075
PALNUT	PS250385
ELMENCO	DM15-C-010-D
ELMENCO	DM15-020-D
ELMENCO	DM15-030-D
ELMENCO	DM15-050-D
ERIE	831-000-C060-509C
ERIE	831-000-C060-100D
ERIE	801-000-C060-150J
ERIE	801-000-C060-220J
ELMENCO	DM15-300J
ERIE	831-000-X5F0-470K
ERIE	831-000-X5F0-680K
ERIE	831-000-X5F0-101K
ERIE	831-000-X5F0-151K
MALLORY	6X320
ERIE	831-000-X5F0-221K
ERIE	831-000-X5F0-331K
ERIE	831-000-X5F0-471K
ELMENCO	DM15-102J
ERIE	CK60AW102M
ERIE	538-006-D9-35

PART NO.	QTY	PRICE	DESCRIPTION
78-01	2	3.10	CAPACITOR TRIMMER 3-15PF
79-01	21	1.86	CAPACITOR TRIMMER 2-8PF
82-03	1	1.80	CAPACITOR 5% .0022UF
93-00	1	.40	CAPACITOR 10% .01UF
93-01	239	.18	CAPACITOR 10% .01UF
94-02	1	1.71	CAPACITOR 20% .01UF
110-01	1	1.65	CAPACITOR 5% .1UF
111-00	2	2.31	CAPACITOR 20% .1UF
116-00	44	.65	CAPACITOR 2UF 50V
131-00	59	.90	CAPACITOR 20% 2.2UF 20V
133-00	17	1.04	CAPACITOR 20% 2.2UF 35V
142-00	6	.65	CAPACITOR 10UF 25V
142-01	10	.68	CAPACITOR 10UF 50V
144-00	6	1.12	CAPACITOR 20% 22UF 15V
145-02	2	1.05	CAPACITOR 50UF 50V
147-01	2	3.38	CAPACITOR 20% 100UF 20V
148-00	1	1.39	CAPACITOR 100UF 25V
157-17	4	3.78	CAPACITOR 13000UF 15V
157-23	4	3.78	CAPACITOR 5500UF 40V
167-00	2	6.40	CONNECTOR 50 SOCKET
169-00	2	8.08	CONNECTOR 75 SOCKET
177-00	1	2.85	CONNECTOR 5 PIN
182-02	1	5.28	CONNECTOR FLANGED INLET
234-02	2	.88	DIODE ZENER 1N5235B
237-00	18	.88	DIODE ZENER 1N5242B
238-00	1	10.00	DIODE ZENER 1N825

MANUFACTURER MANUFACTURER'S PART NO.

ERIE	538-006-D3-15
ERIE	538-006A2-B
ELPAC	B6A222J
ELMENDO	1DF-1-103
ERIE	B05-000-X5V0-103Z
ELPAC	B1A103
ELPAC	B1A104J
SPRAGUE	5C023104X0500B3
CDE	NLW-2-50
SPRAGUE	CS13BE225M
SPRAGUE	CS13BF225M
CDE	NLW-10-25
CDE	NLW-10-50
SPRAGUE	CS13BD226M
CDE	NLW-50-50
SPRAGUE	CS13BE107M
CDE	NLW-100-25
SPRAGUE	36D133B015AC2A
SPRAGUE	36D552G040AC2A
WINCHESTER	MRAC-50S-J6
WINCHESTER	MRAC-75S-J6
CANNON	MS3102A-14S-5P
ARROW-HART	7486
MOTOROLA	1N5235B
MOTOROLA	1N5242B
MOTOROLA	1N825

ASSY PART NO. 58700-00 . . . CONSOLIDATED ASSY PARTS

PART NO.	QTY	PRICE	DESCRIPTION	
239-00	293	.16	DIODE	1N4148
239-01	17	.47	DIODE	1N914B
240-80	6	1.60	DIODE ZENER	1N962B
244-01	1	.80	DIODE	1N4001
244-03	4	.84	DIODE ZENER	1N5223B
244-04	3	.64	DIODE ZENER	1N5221B
244-08	35	.88	DIODE ZENER	1N5232B
244-09	1	.64	DIODE ZENER	1N5230B
244-17	2		DIODE ZENER	1N5260B
246-01	2	6.63	RECTIFIER BRIDGE	MDA952-2
247-20	60	.88	DIODE ZENER	1N5255B
248-06	20	.88	DIODE ZENER	1N5231B
248-07	2	1.04	DIODE ZENER	1N5236B
248-08	1	.64	DIODE ZENER	1N5234B
248-10	12	.88	DIODE ZENER	1N5240B
248-12	8	.88	DIODE ZENER	1N5245B
248-13	24	.64	DIODE ZENER	1N5241B
248-14	2	.64	DIODE ZENER	1N5237B
248-22	31	1.80	DIODE	5082-2B10
248-26	23	1.56	DIODE L.E.D.	135-3510
256-04	1	20.74	FAN	
257-01	2	4.00	FINGER GUARD	
261-02	4	.58	FERRULE HANDLE	
261-14	50	.47	FERRULE TERMASHIELD	
262-00	100	.35	FERRULE	
266-01	1	.76	FUSE 2AMP 3AG SLO-BLO	

MANUFACTURER MANUFACTURER'S PART NO.

HORIZON	1N414B
FAIRCHILD	1N914B
MOTOROLA	1N962B
MOTOROLA	1N4001
MOTOROLA	1N5223B
MOTOROLA	1N5221B
MOTOROLA	1N5232B
MOTOROLA	1N5230B
MOTOROLA	MDA952-2
MOTOROLA	1N5255B
MOTOROLA	1N5231B
MOTOROLA	1N5236B
MOTOROLA	1N5234B
MOTOROLA	1N5240B
MOTOROLA	1N5245B
MOTOROLA	1N5241B
MOTOROLA	1N5237B
HEWLETT PACK	5082-2810
ELDEMA	135-3510
TMC	WS2107FL
PAMOTOR	5504
USECO	904-17
AMP	323932
AMP	323930
LITTLEFUSE	313002

PART NO.	QTY	PRICE	DESCRIPTION	
274-00	1	1.52	FUSEHOLDER	
280-05	2	2.97	HANDLE CABINET	
284-01	25	.56	HEAT SINK	
296-00	34	.23	NUT LOCK 4-40	
297-00	26	.30	NUT LOCK 6-32	
299-00	4	.25	NUT LOCK 10-32	
313-00	4	.10	NUT 8-32	
318-00	15	.07	NUT 4-40	
318-01	62	.01	NUT 4-40	1
326-00	7	.25	TRANSISTOR PAD	
332-00	250	.86	CONTACT SOCKET	
340-22	1	2.55	POTENTIOMETER	50
341-04	1	2.85	POTENTIOMETER	100
342-01	6	2.85	POTENTIOMETER	100
344-07	10	2.70	POTENTIOMETER	500
344-80	6	2.85	POTENTIOMETER	500
345-80	1	2.85	POTENTIOMETER	1K
346-80	8	2.85	POTENTIOMETER	2K
347-01	9	2.85	POTENTIOMETER	2K
351-80	16	2.70	POTENTIOMETER	5K
358-80	13	2.70	POTENTIOMETER	10K
359-03	4	2.85	POTENTIOMETER	10K
360-03	6	3.00	POTENTIOMETER	20K
362-00	1	1.65	POTENTIOMETER	50K
369-02	10	2.70	POTENTIOMETER	50K
372-03	14	2.85	POTENTIOMETER	50K

MANUFACTURER MANUFACTURER'S PART NO.

LITTLEFUSE	342004
USECO	1093-17
IERC	TXBF-032-025B
ANY	NAS679-A04
ANY	NAS679-A06
ANY	NAS679-A3
WALLACE	AN340-CB
WALLACE	NAS-671-C4
COML	
MILTON ROSS	10099-N
WINCHESTER	100-2020S
SPECTROL	43P-500
SPECTROL	62-2-1-101
SPECTROL	43P-101
SPECTROL	43P-501
SPECTROL	62-2-1-501
SPECTROL	43P-102
SPECTROL	62-2-1-202
SPECTROL	43P-202
SPECTROL	62-2-1-502
SPECTROL	62-2-1-103
SPECTROL	43P-103
SPECTROL	62-2-1-203
PRESTON	12004
SPECTROL	62-2-1-503
SPECTROL	43P-503

- ASSY PART NO. 58700-00

CONSOLIDATED ASSY PARTS

PART NO.	QTY.	PRICE	DESCRIPTION
374-02	12	1.71	THERMISTOR 5K
374-04	1	1.80	THERMISTOR 1K
374-05	2	1.65	THERMISTOR 10K
386-03	4	.44	RESISTOR 1/8W 1% 402
387-08	3	.44	RESISTOR 1/8W 1% 1K
387-09	1	.48	RESISTOR 1/8W 1% 1180
388-02	2	.44	RESISTOR 1/8W 1% 3740
389-01	4	.44	RESISTOR 1/8W 1% 4990
389-02	3	.44	RESISTOR 1/8W 1% 5490
390-03	1	.48	RESISTOR 1/8W 1% 6040
390-04	2	.44	RESISTOR 1/8W 1% 7500
392-00	1	.44	RESISTOR 1/8W 1% 20K
392-01	1	.44	RESISTOR 1/8W 1% 24.9K
393-05	2	.44	RESISTOR 1/8W 1% 100K
394-12	2	.48	RESISTOR 1/4W 1% 49.9
394-18	4	.44	RESISTOR 1/4W 1% 71.5
394-22	4	.40	RESISTOR 1/4W 1% 61.9
397-13	3	.44	RESISTOR 1/4W 1% 100
401-04	32	.43	RESISTOR 1/4W 1% 402
402-02	7	.44	RESISTOR 1/4W 1% 499
405-00	14	.44	RESISTOR 1/4W 1% 590
405-01	2	.44	RESISTOR 1/4W 1% 619
407-00	2	.44	RESISTOR 1/4W 1% 750
408-00	3	.43	RESISTOR 1/4W 1% 806
409-00	32	.43	RESISTOR 1/4W 1% 1K
414-00	4	.43	RESISTOR 1/4W 1% 1370

MANUFACTURER MANUFACTURER'S PART NO.

FENWAL	JA-35J1
FENWAL	JB-31J1
FENWAL	JA-41J1
CORNING	NC4-4020-F
CORNING	NC4-1001-F
CORNING	NC4-1181-F
CORNING	NC4-3741-F
CORNING	NC4-4991-F
CORNING	NC4-5491-F
CORNING	NC4-6041-F
CORNING	NC4-7501-F
CORNING	NC4-2002-F
CORNING	NC4-2492-F
CORNING	NC4-1003-F
CORNING	NC5-49R9-F
CORNING	NC5-71R5-F
CORNING	NC5-61R9-F
CORNING	NC5-1000-F
CORNING	NC5-4020-F
CORNING	NC5-4990-F
CORNING	NC5-5900-F
CORNING	NC5-6190-F
CORNING	NC5-7500-F
CORNING	NC5-8060-F
CORNING	NC5-1001-F
CORNING	NC5-1371-F

ASSY PART NO. 58700-00 — CONSOLIDATED ASSY PARTS

PART NO.	QTY	PRICE	DESCRIPTION			
421-00	1	.44	RESISTOR	1/4W	1%	1870
422-00	20	.40	RESISTOR	1/4W	1%	2K
427-00	12	.44	RESISTOR	1/4W	1%	2490
439-01	4	.43	RESISTOR	1/4W	1%	3740
440-00	35	.43	RESISTOR	1/4W	1%	4020
445-00	28	.44	RESISTOR	1/4W	1%	4990
445-01	1	.44	RESISTOR	1/4W	1%	5110
446-00	2	.44	RESISTOR	1/4W	1%	5490
448-00	10	.54	RESISTOR	1/4W	1%	6040
451-06	4	.43	RESISTOR	1/4W	1%	7500
455-03	2	.43	RESISTOR	1/4W	1%	9310
456-03	22	.43	RESISTOR	1/4W	1%	10K
458-01	2	.44	RESISTOR	1/4W	1%	11.5K
459-00	1	.44	RESISTOR	1/4W	1%	12.4K
460-00	1	.43	RESISTOR	1/4W	1%	15K
460-03	8	.72	RESISTOR	1/4W	1%	15.8K
463-00	8	.40	RESISTOR	1/4W	1%	18.2K
465-02	28	.43	RESISTOR	1/4W	1%	20K
467-03	2	.43	RESISTOR	1/4W	1%	24.9K
468-01	3	.44	RESISTOR	1/4W	1%	29.4K
469-00	1	.44	RESISTOR	1/4W	1%	33.2K
469-01	2	.44	RESISTOR	1/4W	1%	34K
471-03	4	.43	RESISTOR	1/4W	1%	40.2K
472-25	10	.43	RESISTOR	1/4W	1%	49.9K
475-02	5	.44	RESISTOR	1/4W	1%	78.7K
478-00	1	.49	RESISTOR	1/4W	1%	100K

MANUFACTURER --- MANUFACTURER'S PART NO.

CORNING	NC5-1871-F
CORNING	NC5-2001-F
CORNING	NC5-2491-F
CORNING	NC5-3741-F
CORNING	NC5-4021-F
CORNING	NC5-4991-F
CORNING	NC5-5111-F
CORNING	NC5-5491-F
CORNING	NC5-6041-F
CORNING	NC5-7501-F
CORNING	NC5-9311-F
CORNING	NC5-1002-F
CORNING	NC5-1152-F
CORNING	NC5-1242-F
CORNING	NC5-1502-F
CORNING	NC5-1582-F
CORNING	NC5-1822-F
CORNING	NC5-2002-F
CORNING	NC5-2492-F
CORNING	NC5-2942-F
CORNING	NC5-3322-F
CORNING	NC5-3402-F
CORNING	NC5-4022-F
CORNING	NC5-4992-F
CORNING	NC5-7872-F
CORNING	NC5-1003-F

ASSY PART NO. 58700-00 - - CONSOLIDATED ASSY PARTS

PART NO.	QTY	PRICE	DESCRIPTION				
478-05	3	.44	RESISTOR	1/4W	1%	154K	
478-16	2	.40	RESISTOR	1/4W	1%	133K	
479-00	13	.43	RESISTOR	1/4W	1%	200K	
484-00	1	.44	RESISTOR	1/4W	1%	499K	
488-11	6	.43	RESISTOR	1/2W	1%	2M	
488-16	15	.43	RESISTOR	1/4W	1%	1M	
494-05	3	.43	RESISTOR	1/2W	1%	806	
495-00	9	.43	RESISTOR	1/2W	1%	1K	
495-06	3	.43	RESISTOR	1/2W	1%	1580	
496-02	3	.44	RESISTOR	1/2W	1%	3160	
496-05	3	.44	RESISTOR	1/2W	1%	3240	
520-00	8	.10	RESISTOR	1/4W	10%	10	
521-00	114	.10	RESISTOR	1/4W	10%	22	
522-00	33	.10	RESISTOR	1/4W	10%	33	
523-00	42	.10	RESISTOR	1/4W	10%	47	
525-00	146	.10	RESISTOR	1/4W	10%	100	
525-03	4	.10	RESISTOR	1/4W	10%	150	
526-00	23	.18	RESISTOR	1/4W	10%	180	
527-00	19	.10	RESISTOR	1/4W	10%	220	
528-00	10	.10	RESISTOR	1/4W	10%	330	
529-00	44	.10	RESISTOR	1/4W	10%	470	
530-00	2	.13	RESISTOR	1/4W	10%	680	
531-00	107	.10	RESISTOR	1/4W	10%	1K	
532-00	2	.10	RESISTOR	1/4W	10%	1500	
533-00	77	.10	RESISTOR	1/4W	10%	2200	
534-00	10	.10	RESISTOR	1/4W	10%	2700	

MANUFACTURER MANUFACTURER'S PART NO.

CORNING NC5-1543-F

CORNING NC5-1333-F

CORNING NC5-2003-F

CORNING NC5-4993-F

CORNING NC6-2004-F

CORNING NC5-1004-F

CORNING NC6-8060-F

CORNING NC6-1001-F

CORNING NC6-1581-F

CORNING NC6-3161-F

CORNING NC6-3241-F

ALLEN-BRADLE CB1001

ALLEN-BRADLE CB2201

ALLEN-BRADLE CB3301

ALLEN-BRADLE CB4701

ALLEN-BRADLE CB1011

ALLEN-BRADLE CB1511

ALLEN-BRADLE CB1611

ALLEN-BRADLE CB2211

ALLEN-BRADLE CB3311

ALLEN-BRADLE CB4711

ALLEN-BRADLE CB6811

ALLEN-BRADLE CB1021

ALLEN-BRADLE CB1521

ALLEN-BRADLE CB2221

ALLEN-BRADLE CB2721

ASSY PART NO. 58700-00

CONSOLIDATED ASSY PARTS

PART NO.	QTY	PRICE	DESCRIPTION		
535-00	29	.20	RESISTOR 1/4W 10%	3300	
536-00	20	.10	RESISTOR 1/4W 10%	4700	
537-00	3	.10	RESISTOR 1/4W 10%	6800	
538-00	78	.10	RESISTOR 1/4W 10%	10K	
540-00	4	.09	RESISTOR 1/4W 10%	15K	
541-00	22	.09	RESISTOR 1/4W 10%	22K	
544-00	11	.10	RESISTOR 1/4W 10%	47K	
546-00	4	.34	RESISTOR 1/4W 10%	68K	
547-00	11	.10	RESISTOR 1/4W 10%	100K	
548-00	1	.10	RESISTOR 1/4W 10%	220K	
551-00	1	.10	RESISTOR 1/4W 10%	1M	
553-00	1	.10	RESISTOR 1/4W 10%	2.2M	
555-00	1	.10	RESISTOR 1/4W 10%	4.7M	
555-01	1	.10	RESISTOR 1/4W 10%	10M	
558-06	8	.19	RESISTOR 1/2W 5%	2	
559-00	2	.10	RESISTOR 1/2W 10%	4.7	
561-00	16	.09	RESISTOR 1/2W 10%	22	
565-00	7	.17	RESISTOR 1/2W 10%	100	
566-00	1	.20	RESISTOR 1/2W 10%	150	
602-09	3	1.71	RESISTOR 3.75W 1%	560	
607-04	8	.26	RESISTOR 2W 10%	100	
608-00	2	1.24	RESISTOR 3W 5%	1	
608-07	1	.84	RESISTOR 3W 5%	2	
609-80	4	1.00	RESISTOR 5W 5%	20	
609-95	1	8.10	RESISTOR 5W 5%	.5	
624-00	16	.05	SCREW FILL 4-40 X 3/8		

MANUFACTURER MANUFACTURER'S PART NO.

ALLEN-BRADLE CB3321

ALLEN-BRADLE CB4721

ALLEN-BRADLE CB6821

ALLEN-BRADLE CB1031

ALLEN-BRADLE CB1531

ALLEN-BRADLE CB2231

ALLEN-BRADLE CB4731

ALLEN-BRADLE CB6831

ALLEN-BRADLE CB1041

ALLEN-BRADLE CB2241

ALLEN-BRADLE CB1051

ALLEN-BRADLE CB2251

ALLEN-BRADLE CB4751

ALLEN-BRADLE CB1061

ALLEN-BRADLE EB2005

ALLEN-BRADLE EB4701

ALLEN-BRADLE EB2201

ALLEN-BRADLE EB1011

ALLEN-BRADLE EB1511

DALE RS-2B

ALLEN-BRADLE HB1011

SPRAGUE 242E1R05

SPRAGUE 450E2R05

SPRAGUE 243E2005

DALE G-5C

ANY AN500D-4-6

PART NO.	QTY	PRICE	DESCRIPTION	
641-00	24	.07	SCREW FHMS 6-32 X 3/8	
655-02	4	.12	SCREW SET 4-40 X 1/8	
659-00	12	.04	SCREW PHMS 2-56 X 5/16	
665-00	19	.04	SCREW PHMS 4-40 X 5/16	
666-00	23	.05	SCREW PHMS 4-40 X 3/8	
668-00	62	.04	SCREW PHMS 4-40 X 1/2	
672-00	4	.08	SCREW PHMS 4-40 X 1	
675-00	2	.06	SCREW PHMS 6-32 X 3/8	
679-00	8	.06	SCREW PHMS 6-32 X 3/4	
700-00	4	.26	SCREW HEX 10-32 X 5/8	
724-00	20	.23	SCREW HEX HD 10-32 X 3/8	
754-01	1	2.65	SWITCH TOGGLE	
756-02	2	3.80	SWITCH PUSHBUTTON	
764-01	14	2.85	SWITCH TOGGLE	
794-00	4	.34	LUG CRIMP	
800-02	1	2.82	THERMOSTAT	
824-00	24	1.40	TRANSISTOR	2N1132
828-00	38	1.08	TRANSISTOR	2N1711
830-01	1	2.07	TRANSISTOR	2N2219
830-02	4	2.60	TRANSISTOR	2N2219A
838-02	5	1.32	TRANSISTOR	2N2905A
838-04	4	5.00	TRANSISTOR	2N2914
842-01	16	.96	TRANSISTOR	2N4264
845-05	8	10.00	TRANSISTOR SELECTED	9932
845-10	17	5.70	TRANSISTOR	E7001
846-00	126	.42	TRANSISTOR	2N3904

MANUFACTURER MANUFACTURER'S PART NO

ANY	AN507C-632-R6
ANY	AN565-D4-H2
ANY	MS35216-4
ANY	MS35216-13
ANY	MS35216-14
ANY	MS35216-16
ANY	MS35216-20
ANY	MS35216-25
ANY	MS35216-29
ANY	TF538C-1032-10
WALLACE	TF538C-1032-6
CUTLER/HAM	B360K7
C&K	PB121-2/DRESS NUT
C&K	7101/DRESSNUT
AMP	318B1
TEXAS INST	20700L79-648L155-2.5
MOTOROLA	2N1132
RAYTHEON	2N1711
NATIONAL	2N2219
NATIONAL	2N2219A
NATIONAL	2N2905A
MOTOROLA	2N2914
MOTOROLA	2N4264
SILICONIX	9932
SILICONIX	E7001
MOTOROLA	2N3904

PART NO.	QTY	PRICE	DESCRIPTION	
846-01	82	.49	TRANSISTOR	2N3906
846-03	6	2.01	TRANSISTOR	2N4921
846-08	32	2.37	TRANSISTOR	2N4939
846-09	1	21.25	TRANSISTOR	2N4016
846-10	11	2.37	TRANSISTOR	2N4918
847-01	13	1.80	TRANSISTOR SELECTED	9934
847-12	7	18.00	TRANSISTOR	2N5516
848-09	1	.96	INTEGRATED CIRCUIT	74H30
848-12	8	1.84	INTEGRATED CIRCUIT	74H40
848-14	14	1.53	INTEGRATED CIRCUIT	74H00
848-15	1	8.75	INTEGRATED CIRCUIT	74154
848-17	2	7.05	INTEGRATED CIRCUIT	74155
848-23	3	2.07	INTEGRATED CIRCUIT	MC3026P
848-24	28	1.44	INTEGRATED CIRCUIT	74H50
848-27	5	4.25	INTEGRATED CIRCUIT	7475
848-32	1	2.95	INTEGRATED CIRCUIT	CA3019
848-33	2	.27	INTEGRATED CIRCUIT	MC1709CG
848-40	7	2.01	INTEGRATED CIRCUIT	74H04
848-48	18	1.52	INTEGRATED CIRCUIT	74H10
848-58	6	5.25	INTEGRATED CIRCUIT	74157
848-59	2	7.30	INTEGRATED CIRCUIT	74161
848-60	2	2.58	INTEGRATED CIRCUIT	7486
848-98	10	2.34	INTEGRATED CIRCUIT	8601
849-18	1		INTEGRATED CIRCUIT	MC1741SC6
849-19	1		INTEGRATED CIRCUIT	LH0002CH
851-00	1	.05	WASHER I.T. 3/8	

MANUFACTURER MANUFACTURER'S PART NO.

MOTOROLA	2N3906
MOTOROLA	2N4921
MOTOROLA	2N4939
MOTOROLA	2N4016
MOTOROLA	2N4918
UNION CARBID	9934
SILICONIX	2N5516
ANY	74H30 (PLASTIC)
ANY	74H40 (PLASTIC)
ANY	74H00 (PLASTIC)
ANY	74154 (ALT 9311)
ANY	74155 (PLASTIC)
MOTOROLA	MC3026P (PLASTIC)
ANY	74H50 (PLASTIC)
ANY	7475 (PLASTIC)
RCA	CA3019 (MT CAN)
MOTOROLA	MC1709CG (MT CAN)
ANY	74H04 (PLASTIC)
ANY	74H10 (PLASTIC)
ANY	74157 (ALT 9322)
ANY	74161 (ALT 9316)
ANY	7486 (PLASTIC)
ANY	8601 (ALT 9601)
MOTOROLA	MC1741SCG (MT CAN)
NATIONAL	LH0002CH (MT CAN)
SMITH	1145

PART NO.	QTY	PRICE	DESCRIPTION
854-00	25	.02	WASHER FLAT #6 SM
855-00	122	.02	WASHER FLAT #4 SM
857-02	6	.04	WASHER FLAT #4 FIBRE
859-00	5	.09	WASHER SHOULDER #4 NYLON
859-01	1	.10	WASHER SHOULDER BUSHING NYLON
859-02	5	.15	WASHER SHOULDER NYLON
863-00	1	.01	WASHER E.T. #6
863-02	1	.01	WASHER E.T. #8
864-00	16	.01	WASHER E.T. # 10
869-00	8	.03	WASHER FLAT #6 STD
871-00	4	.01	WASHER FLAT #8
872-00	8	.05	WASHER FLAT #10
874-00	76	.02	WASHER LOCK #4
876-00	3	.02	WASHER LOCK #8
877-00	4	.02	WASHER LOCK #10
972-01	1	25.10	CHASSIS SLIDE
998-07	4	9.93	RESISTOR .02% 796
998-10	16	9.00	RESISTOR .02% 1K
998-15	2	2.37	RESISTOR .02% 1593.4
998-16	4	6.00	RESISTOR .02% 1587.7
998-20	5	2.37	RESISTOR .02% 1996
998-24	4	6.00	RESISTOR .02% 3160
998-25	20	2.37	RESISTOR .02% 3988.4
998-26	4	6.00	RESISTOR .02% 3200
998-30	3	5.75	RESISTOR .02% 3992.4
998-42	2	10.85	RESISTOR .02% 4084

MANUFACTURER MANUFACTURER'S PART NO.

WALLACE	NAS 620-C6
WALLACE	NAS 620-C4
SEASTROM	5602-10-32
SEASTROM	5607-10
BENDIX	2106307
SEASTROM	5607-11
WALLACE	AN936-B6
WALLACE	AN936-B8
WALLACE	AN936-B10
WALLACE	AN960-C6
WALLACE	AN960-CBL
WALLACE	AN960-C10L
WALLACE	MS35337-78
WALLACE	MS35337-80
WALLACE	MS35337-81
ZERO MFG	C-300S-16 E98
VISHAY	V53-1-796
VISHAY	V53-1-1K
VISHAY	V53-1-1593.4
VISHAY	V53-1-1587.7
VISHAY	V53-1-1996
VISHAY	V53-1-3160
VISHAY	V53-1-3988.4
VISHAY	V53-1-3200
VISHAY	V53-1-3992.4
VISHAY	V53-1-4084

PART NO.	QTY	PRICE	DESCRIPTION	
998-45	4	2.37	RESISTOR .02%	7920.4
998-46	6	2.37	RESISTOR .02%	7993.6
998-53	2	9.00	RESISTOR .02%	10K
998-70	2	8.38	RESISTOR .02%	20K
998-80	1	5.00	RESISTOR .02%	413
9922-00	14	1.40	TRANSISTOR SELECT	A
9944-00	8	4.75	TRANSISTOR SELECT PAIR	A
9946-00	16	1.92	TRANSISTOR SELECT	A
12018-01	1	.35	SHAFT EXTENDER	B
12027-00	1	.44	BRACE SINGLE POTENTIOMETER	B
30051-03	2	1.77	KNOB CONTROL	C
31818-00	1	1.32	BUSHING	B
40341-00	62	.45	GUIDE CARD	D
40454-00	2	10.00	COVER SIDE RIGHT & LEFT	D
40455-00	2	9.55	COVER TOP & BOTTOM	D
40456-02	1	10.00	PANEL REAR 2 AMP	A
40457-00	4	3.75	SUPPORT INTERCONNECT	C
40461-00	23	.31	LENS LAMP	C
40461-02	1	.15	PLUG LAMP	C
40475-00	2	.15	PLUG SWITCH	C
46019-00	4	11.25	D&R ASSY AMP LOGIC B	C
46020-00	2	7.85	SHIELD COMPONENT SIDE	C
46021-00	3	6.50	SHIELD CIRCUIT SIDE	B
46026-00	3	13.75	D&R ASSY AMP LOGIC C	C
46027-00	1	30.80	TRANSFORMER ASSY	C
46079-00	9	.80	HEATSINK	A

MANUFACTURER	MANUFACTURER'S PART NO.
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VISHAY	V53-1-7920.4
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VISHAY	V53-1-7993.6
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VISHAY	V53-1-10K
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VISHAY	V53-1-20K
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VISHAY	V53-1-413
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PART NO.	QTY	PRICE	DESCRIPTION		
46128-00	1	11.25	D&R	ASSY 4 BIT AMP	C
46178-00	1	11.25	D&R	ASSY 4 BIT LOGIC	C
46203-00	1		D&R	ASSY AMP LOGIC A	C
48088-00	1	30.00	D&R	ASSY INTERCONN PWR SUP	C
48229-00	1	3.00		THERMOSTAT BRACKET	A
51875-00	4	2.50		HEAT SINK	B
52094-01	1	2.40		SHIELD PLATE	A
52099-00	1	3.75		TRANSFORMER ASSY	B
52184-00	1	7.85		SHIELD COMPONENT SIDE	C
52383-00	1		D&R	ASSY GMSH	C
52528-00	2	13.75	D&R	ASSY 4 CHANNEL MUX	C
52533-00	1	13.75	D&R	ASSY MUX COUNTER REG	C
52538-00	1	13.75	D&R	ASSY ADC CONTROL	C
52543-00	1	13.75	D&R	ASSY MUX CONTROL	C
52548-00	1	13.75	D&R	ASSY MUX DECODE 128 CHAN	C
52582-00	2	2.64		SWITCH ASSY MODE	A
55742-00	1	2.40		FEED THRU TERMINAL ASSY	B
56497-00	1	13.75	D&R	ASSY GUARD DRIVER	C
56623-00	3	13.75	D&R	ASSY AMP LOGIC A	C
58168-00	1	7.50	D&R	ASSY LAMP DRIVER MUX	C
58693-00	1	10.00	D&R	ASSY LAMP DRIVER ADC	C
58705-00	1			PLATE CONNECTOR	B
58707-00	1		D&R	ASSY INTERCONNECT BD A	C
58709-00	1		D&R	ASSY INTERCONNECT BD C	C
58713-00	1	13.75	D&R	ASSY SIGN STORAGE	C
58718-00	1	13.75	D&R	ASSY GMD AMP MUX	C

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<u>MANUFACTURER</u>	<u>MANUFACTURER'S PART NO.</u>
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ASSY PART NO. 58700-00

CONSOLIDATED ASSY PART

PART NO.	QTY	PRICE	DESCRIPTION			
58723-00	2	13.75	D&R	ASSY GMD MUX AMPLIFIER	C	
58968-00	2		D&R	ASSY MUX CONTROL STORAGE	C	
59328-00	1	2.50	D&R	ASSY TRANSISTOR 2N5516	AP	
59329-00	1	1.80		CAN TRANSISTOR	A	
59658-00	1	11.25	D&R	ASSY REF SUPPLIES	C	
59999-21	1			PANEL FRONT GMAD-1	D	
17-00	1	2.76		CLAMP CABLE		
171-00	2	15.20		CONNECTOR 75 PIN HOODED		
187-00	2	18.35		CONNECTOR 50 PIN HOODED		
191-00	1	5.83		CONNECTOR 5 SOCKET		
331-00	250	.44		CONTACT PIN		
48079-00	1	8.03		CABLE ASSY POWER	A	
48289-00	1	18.75	D&R	ASSY EXTENDER	C	
52330-00	1			P.C. ASSY SIGNAL BD EXTENDER	AP	

WINCHESTER 100-2020P

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LIST OF DRAWINGS

58700	Top Assembly
58701	Customer Connection
58702	Wire List
58707	Interconnect Board A
58709	Interconnect Board C
46016	Amp/Logic B
46017	Schematic
46023	Amp/Logic C
46024	Schematic
46125	4 Bit Amp
46126	Schematic
46175	4 Bit Logic
46176	Schematic
46200	Amp/Logic "A"
46201	Schematic
48085-36	Power Supply
58809	Schematic
52380-14	GMSH
52381	Schematic
52525	4 Channel MUX
52526	Schematic
52530	MUX Counter Reg.
52531	Schematic
52535	Schematic

(continued)

52540	MUX Control
52541	Schematic
52545	MUX Decode 128 Channel
52546	Schematic
56494	Guard Driver
56495	Schematic
56620	Amp/Logic A
56621	Schematic
58165-01	Lamp Driver MUX
58166	Schematic
58690	Lamp Driver ADC
58691	Schematic
58710	Sign Storage
58711	Schematic
58715	GMD-100 Amp MUX
58716	Schematic
58720	MUX Amplifier
58721	Schematic
58965	MUX Control Storage
58966	Schematic
59655	Reference Supplies
59656	Schematic

SECTION 9

DRAWINGS

Due to the size of the drawing package, the drawings describing the Part Number **58700** Series Analog-to-Digital Conversion System are bound under separate cover



SCIENTIFIC INCORPORATED
805 East Cerritos Ave., Anaheim, Calif. 92805
Tel. (714) 776-6400 TELEX 65-5321

MODEL GMAD-1

TEST REPORT

Test Technician L. GUARD

Date 5-13-74

Serial Number RAA 434

Register Number 13759

1.0 Assembly number 58700

2.0 Resolution 14 BITS + SIGN

3.0 Output code 2's Comp

4.0 Output level for "1" +3V

5.0 Fullscale input $\pm 10.24V$ AND $\pm 0.1024V$

6.0 Number of counts $\pm 16,384$

7.0 Setup:

SEE TIMING DIAGRAM

(d) Delay# _____
_____ nano/microseconds

(a) +10 volt reference $\pm 10.0014V$ (e) Delay# _____
_____ nano/microseconds

(b) Trigger slope POSITIVE (f) Delay# _____
_____ nano/microseconds

(c) Trigger level $\pm 3V$

8.0 Conversion time 4.1 μ SEC (1.9 μ s USING 2.0)

9.0 Throughput rate 3.5 μ SEC (2 μ SEC USING DTADC)

$\pm 0.025\% \pm 1/2$ LSB (GMM)
10.0 Accuracy $\pm 0.030\% \pm 1/2$ LSB (GMD-1)
 $\pm 0.055\% \pm 1/2$ LSB (GMD-100)

11.0 Crossover check OK

MODEL GMAD — 1
 14 Bits & Sign
 .1024v Full Scale
 RAA 434

ADC TEST REPORT (continued)

Page 2

12.0	BINARY DISPALY	THEORETICAL ANALOG INPUT $\pm .056$ mv	Actual Analog Inputs	Error — Theoretical Minus Actual — IN mv
	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	+0.102394	.102389	— .005
	0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	+0.096000	.096018	+ .018
	0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	+0.089600	.089622	+ .022
	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	+0.076800	.076824	+ .024
	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	+0.051200	.051212	+ .012
	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	+0.012800	.012796	— .004
	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	+0.006400	.006393	— .007
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	+0.000012	—	—
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.000000	— .000005	— .005
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	—0.000006	—	—
	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	—0.006400	.006393	+ .007
	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	—0.012800	.012792	+ .008
	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	—0.025600	.025597	+ .003
	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	—0.051200	.051205	— .005
	1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	—0.076800	.076806	— .006
	1 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	—0.089600	.089601	— .001
	1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	—0.096000	.095998	+ .002
	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	—0.102394	.102385	+ .009

13.0 First reading error and crosstalk LESS THAN 9 COUNTS

READINGS TAKEN ON CHAN 1 (GMD-100)

14 Bits & Sign

10.24v Full Scale

RAA 434

12.0	Binary Display (2's Complement)	Theoretical Analog Input ± 3.1 mv	Actual Analog Inputs	Error-Theoretical Minus Actual - IN mv
	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	+ 10.2394	10.2397	+ .3
	0 1 1 1 1 0 0 0 0 0 0 0 0 0 0	+ 9.6000	9.6014	+ .4
	0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	+ 8.9600	8.9612	+ .2
	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0	+ 7.6800	7.6808	+ .8
	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	+ 5.1200	5.1206	+ .6
	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	+ 1.2800	1.2796	-.4
	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	+ .6400	0.6397	-.3
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	+ 0.0012	0.0013	+ .1
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.0000	+0.0004	+ .4
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- 0.0006	0.0000	+ .6
	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0	- .6400	0.6388	+1.2
	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	- 1.2800	1.2787	+1.3
	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	- 2.5600	2.5587	+1.3
	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	- 5.1200	5.1193	+ .7
	1 0 1 0 0 0 0 0 0 0 0 0 0 0 0	- 7.6800	7.6792	+ .8
	1 0 0 1 0 0 0 0 0 0 0 0 0 0 0	- 8.9600	8.9591	+ .9
	1 0 0 0 1 0 0 0 0 0 0 0 0 0 0	- 9.6000	9.5995	+ .5
	1 0 0 0 0 0 0 0 0 0 0 0 0 0 1	- 10.2394	10.2384	+1.0

13.0 First reading error and crosstalk LESS THAN ± 5.4 COUNTS

READINGS TAKEN ON CHAN 3 (GMD-1)

14 Bits & Sign

10.24v Full Scale

RAA 434

12.0	Binary Display (2's Complement)	Theoretical Analog Input ± 2.9 mv	Actual Analog Inputs	Error-Theoretical Minus Actual - (N)
	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	+ 10.2394	10.387	-.7
	0 1 1 1 1 0 0 0 0 0 0 0 0 0 0	+ 9.6000	9.6003	+.3
	0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	+ 8.9600	8.9605	+.5
	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0	+ 7.6800	7.6805	+.5
	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	+ 5.1200	5.1206	+.6
	0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	+ 1.2800	1.2806	+.6
	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	+ .6400	0.6408	+.8
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	+ 0.0012	10.0014	+.2
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0.0000	-0.0001	-.1
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- 0.0006	-0.0003	+.3
	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0	- .6400	0.6393	+.7
	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	- 1.2800	1.2792	+.8
	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0	- 2.5600	2.5594	+.6
	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	- 5.1200	5.1201	-.1
	1 0 1 0 0 0 0 0 0 0 0 0 0 0 0	- 7.6800	7.6803	-.3
	1 0 0 1 0 0 0 0 0 0 0 0 0 0 0	- 8.9600	8.9603	-.3
	1 0 0 0 1 0 0 0 0 0 0 0 0 0 0	- 9.6000	9.6003	-.3
	1 0 0 0 0 0 0 0 0 0 0 0 0 0 1	- 10.2394	10.2389	+.5

13.0 First reading error and crosstalk LESS 10.2394 +.5 counts

READINGS TAKEN ON CHAN 6 (GMM)

CLOCK

TADC
HOLD COMM.

GATE #1

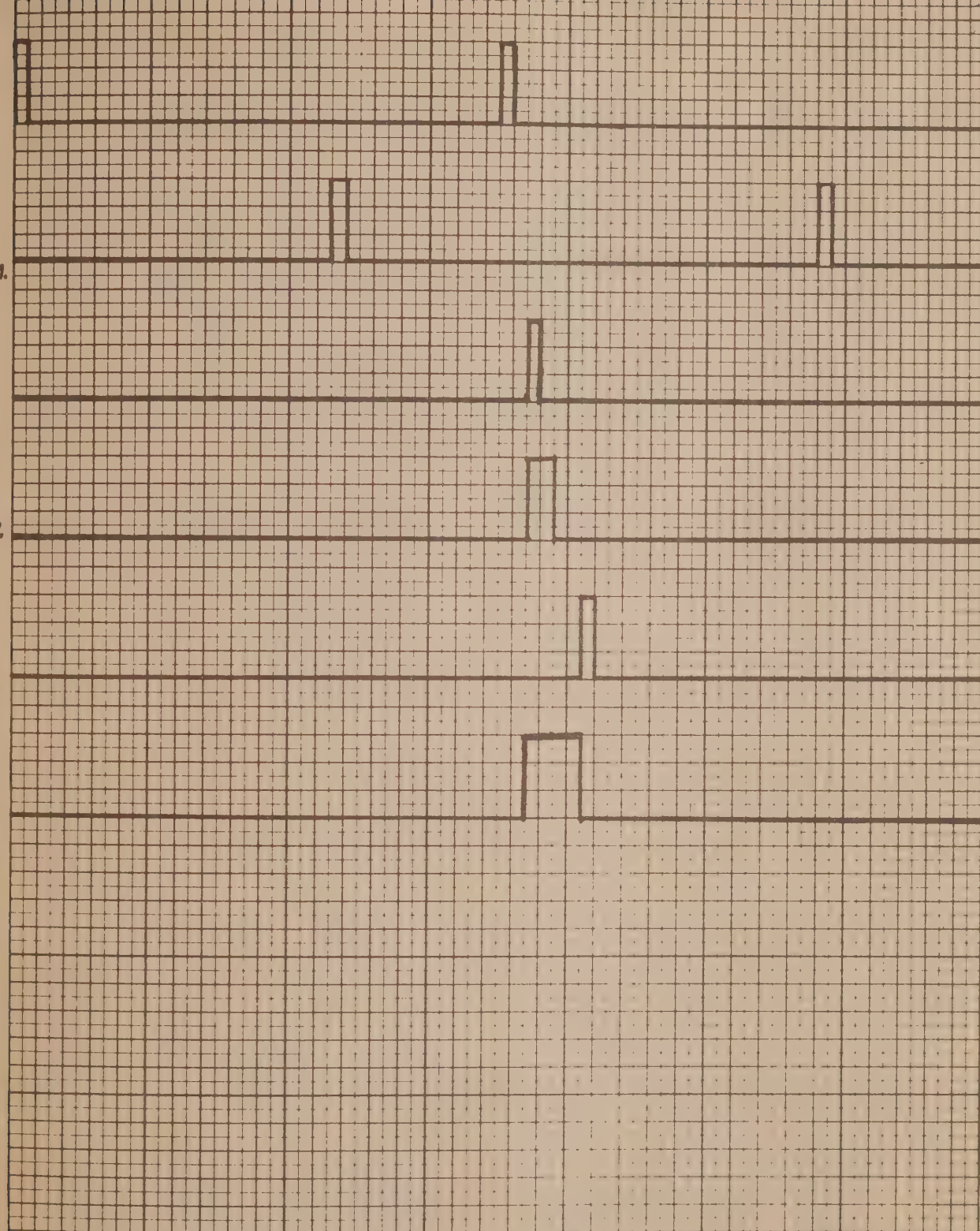
SWAP
COMM.
GATE #2

E.O.C.

BUSY

1 μ SEC. / INCH

RAA 434



DTADC

HOLD COM.
TADC

GATE #1

SAMPLE
COM.
GATE #2

E.O.C.

BUSY

1 μ SEC. / INCH

RAA 434

